

The History

The Specifics

The Capabilities

The Present

The Advantages

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The History An Evolving Laboratory

"The great thing about the Microlab is the way it evolves."

UC Berkeley EECS Professor, William G. Oldham



... from Nanoscale Research to Gigascale Engineering...

The History: Phase 1 Early ICs

Faculty from EE <u>share equipment</u> to be able to conduct research in the new field of integrated circuits

THE EVOLUTION OF THE BERKELEY MICROLAB

Semiconductor Integrated Circuits Fabrication Laboratory, "The Old Lab" 1962 - 1982

In 1960, only months after some of the key patents on integrated circuit fabrication were filed, professors in the department of Electrical Engineering conceived plans for the country's first university IC lab. Working circuits, aligned by hand and fabricated on 3/4-inch-diameter silicon wafers emerged in 1962. As EECS Professor Emeritus David Hodges notes, *"It was pretty primitive in those days . . . but we got some working circuits . . . and we learned an awful lot!"*

Background: N-MOS op-amp. K. Burns/Prof. Paul Gray, 1976



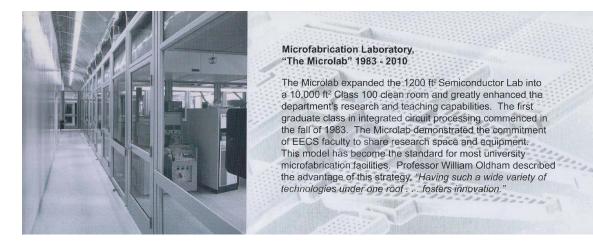
Fabricated some of the earliest fundamental microelectronic devices high speed A/D converters, operational amplifiers

PABX line finder circuit (private automated branch exchange) - the basis of integrated services digital networks



The History: Phase 2, EECS to COE ICs to MEMS to new discrete devices

The shared equipment model is expanded, the faculty base grows, the recharge model is established, and external use is opened.



Home of the First NSF/Industry University Cooperative Research Center (IUCRC) The Berkeley Sensor and Actuator Center BSAC Fabricated some of the first MicroElecroMechanical Systems (MEMS) polysilicon based accelerometers, the basis of the airbag sensor, electrostatically actuated micromotors IC processed piezoelectric microphones The world's smallest (Year 2000) gate length transistor (15nm) One of the first finFET 3D transistors

The History: Phase 3, a cross campus facility Integrating Multiple Technologies

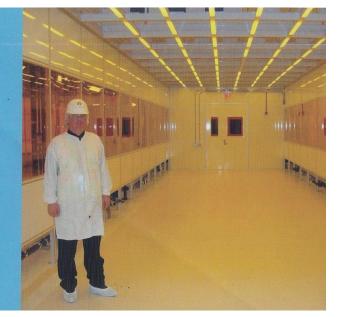
A larger purpose built cleanroom is built after critical mass achieved; commercial use growing to 50% of cost recovery, but 25% of use

Marvell Nanofabrication Laboratory, "The Marvell NanoLab" 2009 -

The Marvell Nanolab is the next stage in Berkeley's shared laboratory evolution. It will provide 15,000 ft² of flexible Class 100 and Class 1000 clean room and support the broadest spectrum of nanotechnology research and education. The Marvell Nanolab is part of the new, multi-campus Center for Information Technology Research in the Interest of Society (CITRIS) initiative.

The formidable challenge before us is to move the entire operation from its home of more than 45 years in Cory Hall to the CITRIS headquarters, Sutardja Dai Hall. It is heartening that so many faculty, staff and friends recognize and support the importance of this enabling lab. Thank you to all who have contributed.

> Under construction: a lithography bay of the new Marvell Nanolab with filtered yellow light for handling photo sensitive material



World's smallest laser (2009) (Xiang Zhang, MechEng) First demonstration of negative capacitance (Sayeef Salahuddin, EECS) Development of nanomechanical transistor relays (Tsu-Jae King Liu, EECS)



The Specifics

- 15,000 ft² (1400 m²) Class 100 Clean Room
- \$5M/year operating budget. 100% recharge recovery
 >50% from industry access affiliate program
- 80 Academic PIs; ~350 researchers/year ~24 companies ; 80 researchers/year 50,000 total use hours/year
- Enabling >\$40M/year in research funds



- The NanoLab provides research capabilities for faculty system wide. An efficiently run shared facility with a low barrier to entry.
- Affiliate program supporting many local startups .

The Capabilities

Lithography

Contact aligners, i-line and 248nm stepper, backside capable, 130 kV e-beam to 7nm, 7 coat /develop tracks, UV hard bake

Deposition

ALD, PECVD, LPCVD: SiO2, Si3N4, poly-Si and SiGe, epi Si and Ge Unique: LACVD, SiC, AlN, diamond, Mo, Ru, 6 evap, 7 sputter

Etch

16 plasma systems including DRIE Si, ICP 3/5, ICP metal, XeF2, HF vapor, KOH, TMAH, Critical Point Drying

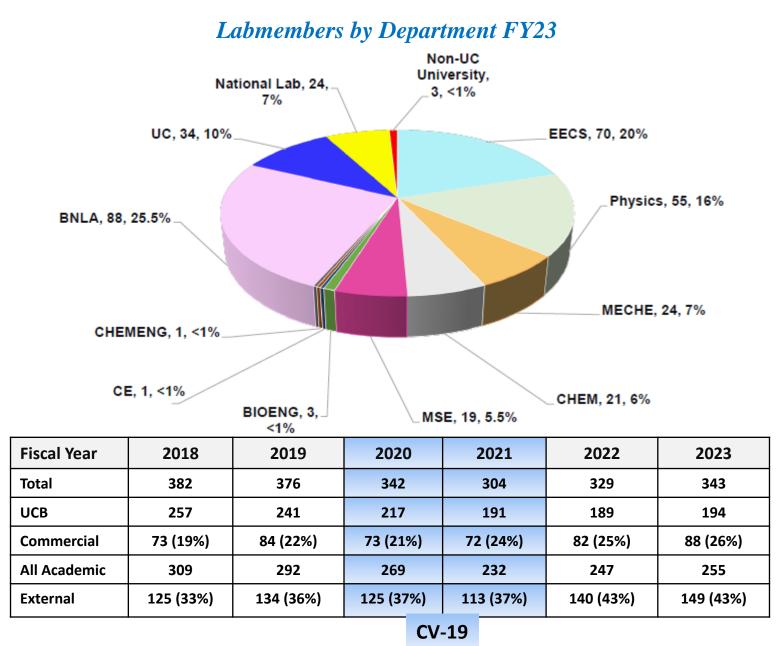
Planarize, Package

Si, SiO2, metal CMP; dicing, wafer bond, flip chip bond, die bond, Au and Al wire bond, parylene encapsulation

Metrology

SEM, AFM, XRD, EDX, reflectometer, contact + optical profilometer, interferometer, FTIR, spectroscopic ellipsometer, Raman scope

Membership is Strong and Stable



An active affiliate company program



Jan 2023: 26 Members

Advantages for Academic Researchers

- More efficient use of valuable laboratory space and specialized research equipment
- Significant improvement in quality of support; researchers focus upon results not maintenance
- Maximum PI research flexibility integrating strategically selected, diverse cutting edge capabilities around a stable silicon baseline
- Wide diversity of research leads to enhanced research cross fertilization
 - Earliest possible interaction with start up companies

Advantages for a VC funded startup

- Cleanroom with wide range of process equipment is immediately available.
- 5 photoresist systems characterized and maintained Immediate mask making capability
- No application and wait for city and county chemical handling permits
- Compare multiple technologies prior to equip purchase
- Well defined research expenses during prototype phase
- Facility access agreement only
 - Ensures separate IP and no revenue or equity sharing

For any Lab related questions, please contact:

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