0.35 μm CMOS PROCESS ON SIX-INCH WAFERS

Baseline Report IV.

A. Horvath, S. Parsa, H.Y. Wong

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Abstract

After the success of our first 6-inch run, CMOS150, which transferred our 4-inch, 1 μm CMOS baseline process to six-inch substrates, we were confident to embark on developing a more aggressive, 0.35μm CMOS baseline process. This, a moderately complex process, includes additional steps, such as silicided source drain, LDD spacers, thinner oxide, RTA and CMP. The first run with the new process, CMOS 161, completed in December 2004, yielded well. The work presented here encompasses our 0.35μm process development work, process simulation, and parametric test results. We also established design rules which will be applied to future CMOS baseline runs.

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1. INTRODUCTION

The Microfabrication Laboratory at the University of California, Berkeley has been supporting silicon MOS technology from the time the present VLSI facility was opened in 1983 [1,2]. The first CMOS baseline report [3] described a 2µm, n-well, double poly-Si, and double metal CMOS process. This process was subsequently developed into a twin-well, 1.3µm, double poly-Si, double metal process. The latter was further refined to produce 1µm transistors on four-inch substrates, report [4]. The same process was also used for the fabrication of our first six-inch run (CMOS150), which played an important role in releasing six-inch equipment/processes in the Microlab. Electrical (parametric) test results, comparable to the previous four-inch runs were realized, which confirmed that the six-inch conversion project was a success, report [5].

The CMOS baseline has always specified standard process modules for VLSI operations, provided test circuits, and a starting point for various research groups such as Berkeley Sensor and Actuator Center (BSAC), Berkeley Computer Aided Manufacturing group, and Berkeley Microfabrication Laboratory affiliates [6, 7, 8]. The baseline runs, in conjunction with in-line equipment monitoring of equipment, have provided an excellent means for staff to quickly discover/address possible equipment/process problems in the Microlab. These baseline runs have also played an important role in releasing new and upgraded tools, as well as pushing out the performance of the high-end equipment in the Microlab. These are some of the reasons why baseline test chips have been continuously fabricated in the Microlab.

CMOS baseline runs had been processed regularly on 4 inch wafers up until 2001; then the first six-inch run (CMOS 150) successfully transferred the old 1 µm baseline onto six-inch wafers. This run was followed by a new and more advanced, 0.35 µm process, which produced the first sub-half micron devices (CMOS161). This run not only established our new 0.35 µm process, but also helped us to push out the performance of some of our tools to more advanced processes. This report includes process development work, which included short loop test runs, as well as the simulation work and parametric test results for the latest six-inch run (CMOS161).

2. PROCESS DEVELOPMENT AND CHARACTERIZATION – SHORT LOOPS

During the past couple of years, process staff have been working on developing a new 0.35 μm process. This work consisted of a total revamp of our previous 1 μm process with new/additional process modules as part of the new process flow. Also highlighted by this change were device physical issues that had to be addressed, to include "hot electron" and "short channel effects" caused by a major scale-down of devices. The new process utilizes poly gate engineering to dope separately the poly-silicon gate material of p-channel and n-channel devices; it also includes additional source/drain ion implants for a lightly doped drain structure (LDD), source/drain spacers, a thinner gate oxide, rapid thermal annealing (RTA) and chemical-mechanical polishing (CMP) steps. Ample amount of process simulations and a few short loop experiments had to be conducted in preparation for the fabrication of the first 0.35μm CMOS run (CMOS161) in the Microlab. The short loop runs characterized the new process modules, also confirmed computer-based process simulation results, which had to be on target, before investing considerable amount of time on the fabrication of the complete run. The observations made through these short loops led to a successful 0.35μm baseline run, completed in December 2004.

2.1 Lightly doped drain (LDD) structure and polysilicon sidewall spacer formation

Several short loop experiments were conducted to determine the exact LDD implant condition and spacer size/shape needed for the fabrication of small-geometry transistors. As device dimensions are reduced, if voltage levels are not correspondingly scaled down, electric fields inside the devices will rise, resulting in high energy ("hot") electrons (or holes) in the channel region. Such high energy carriers can cause impact ionization and easily be injected into the gate dielectric resulting in device reliability problems.

One of the innovations that is almost universally used to address this problem is the Lightly Doped Drain or LDD structure. The idea behind this structure is to grade the doping in the drain region in the vicinity of the channel (an N+N-P profile between the drain and the channel in the NMOS devices and a corresponding P+P-N profile in the PMOS devices). This reduces the peak value of the electric field in the near drain region, and also provides shallow junctions adjacent to the channel, which is less susceptible to “short channel effects”.

Fabrication of the LDD structure and source drain junctions, post polysilicon gate formation, consists of several process steps, as follows:

a. P-type S/D lithography
b. P-type LDD implant (to form the P- lightly doped area across the entire P S/D region)
c. N-type S/D lithography
d. N-type LDD implant (to form the N- lightly doped area across the entire N S/D region)
e. Conformal LPCVD oxide deposition
f. Sidewall spacer formation by anisotropic plasma etch
g. P-type S/D lithography
h. P+ S/D implant (sidewall spacers keep the area hidden from this P+ implant adjacent to the channel along both sides of the polysilicon gate)
i. N-type S/D lithography
j. N+ S/D implant (sidewall spacers keep the area hidden from this N+ implant adjacent to the channel along both sides of the polysilicon gate)

LDD implants

Implant dose and energy needed to be selected carefully and controlled to produce a desired graded drain junction. BF_2 implant at 20KeV and dose of 1E14 was used to form the P-type shallow junctions for the CMOS 161 run, while As^+ implant with 1E14 dose at 30KeV was used for the N-type devices. Both implants were done at 7˚ tilt (wafer orientation of 0˚ and 180˚) to place the implant further under the edge of the gate.

CVD oxide deposition, sidewall spacer formation

Conformal deposition of the dielectric material plays an important role in the sidewall spacer formation. The thickness of this layer will determine the width of the sidewall spacer region, and if chosen properly, can optimize device characteristics. The effect of different spacer widths on transistor characteristics were evaluated through computer simulation, where optimum width was determined to be in the target range of 2500Å - 3000Å for the best device performance. This required deposition of approximately 4000Å thick TEOS (oxide) layer in our P5000 system (AMAT). TEOS CVD oxide deposition was chosen over silane-based films, due to its more conformal step coverage and superior wafer to wafer thickness uniformity.

A Centura system (AMAT) with its MxP^{+} etch chamber was used to perform an anisotropic etch on the deposited TEOS layer, which resulted in the desired spacer shape/width shown in Figure 1. The endpoint capability available on this advanced tool was also helpful in protecting the source drain areas and in clearing out any remaining TEOS film from the top area of the electrode. This means, TEOS oxide was removed everywhere except along the edges of the vertical steps (spacer) in the underlying structures.

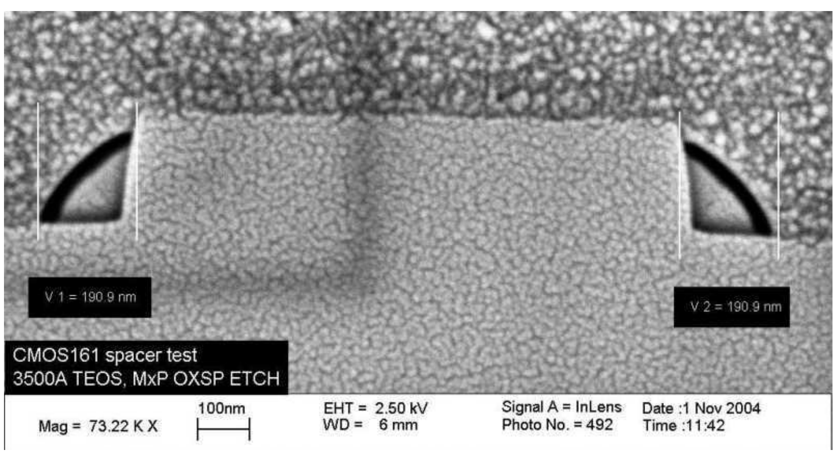


Fig. 1 - SEM cross-section of a sample prepared for sidewall spacer analysis

2.2 Titanium silicide formation

Self-aligned titanium silicide ($TiSi_2$) was formed on source, drain and gate areas to enable low sheet and contact resistances. The silicidation process consisted of the following process steps after the source and drain regions were formed:

a. 300Å Ti sputtering
b. Rapid Thermal Annealing (RTA) at 650˚C for 15 sec in nitrogen atmosphere
c. Removal of TiN film formed by the anneal process, and un-reacted Ti layer, in piranha
d. Rapid Thermal Annealing (RTA) at 900˚C for 10 sec in nitrogen atmosphere

As can be seen above, the formation of low resistivity silicide layers requires two separate thermal cycles. During the first cycle a higher resistivity layer is formed (TiSi); then a higher temperature cure (2nd cycle) completes the silicidation process, resulting in a final low resistivity $TiSi_2$ layer. This process sequence will generate a TiN layer, which is formed during the first annealing step in nitrogen ambient. This TiN layer along with and any excess (un-reacted) Ti material will need to be removed to complete the titanium silicidation process. Piranha is a convenient way to get rid of these excess materials, while the desired $TiSi_2$ layer remains untouched. The sheet resistance value of our titanium silicide ($TiSi_2$) layer was below10 Ω/square.

2.3 Contact/via, spacer etch process development

An advanced Applied Materials (AMAT) etcher (Centura) became available to us in 2003, just in time for the contact etch step of the CMOS161 run. This run required a better oxide etcher than previous runs because of its smaller contact/via sizes. This multi-chamber machine offered oxide and nitride etch capabilities in its MxP^+ chamber. SEM pictures of 0.35 µm and 1 µm contact holes etched in this chamber are shown in Figure 2. The process was optimized at the following conditions:

Oxide etch recipe: 200 mT/700W/30Gauss
45sccmCHF3/15sccmCF4/150sccmAr

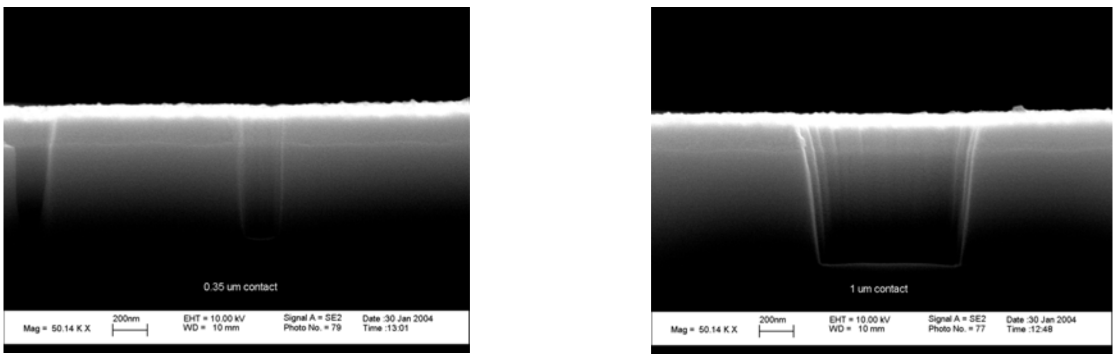
Oxide etch rate: 4413 Å/min

Uniformity: 3.9%

Oxide to poly selectivity – 9:1

Oxide to nitride selectivity – 2:1

Oxide to DUV photoresist selectivity – 5:1



(a) (b)

Fig. 2 - SEM cross section of 0.35µm (a) and 1µm (b) contact holes etched in 1.5µm thick LTO Lithography was done on ASML 5500/90, and etch was done in Centura MxP+

The above recipe was modified to fulfill the process requirements of the oxide sidewall spacer formation, which included higher oxide to silicon selectivity, slower and more directional etch. The new recipe combined with the "etch to endpoint" feature provided optimal conditions for the oxide spacer etch process. Fig.1 shows SEM sidewall image of the spacer structure etched in the Centura MxP$^+$ chamber, by utilizing our final spacer etch recipe, listed below:

Oxide spacer etch recipe: 200mT/500W/30Gauss
50sccmCHF3/10sccmCF4/120sccmAr

Oxide etch rate: 3100 Å/min

Uniformity: 3.2%

Oxide to silicon selectivity – 11:1

Oxide to nitride selectivity – 2.5:1

Oxide to DUV photoresist selectivity – 9:1

3. CMOS BASELINE FABRICATION PROCESS

The first six-inch CMOS baseline run addressing the 0.35µm technology node was completed in December 2004. This latest run was named "CMOS161". A moderately complex 0.35µm twin-well, silicided process was developed to meet certain design specifications, with the Microlab's tool capabilities/limitations in mind. Iterative computer simulation and feedbacks from short loop runs were used to optimize the new 0.35µm process prior to fabrication. The final version of 0.35µm process consists of 51 individual steps, after which N-channel and P-channel MOSFET devices, as well as some simple circuits were functional. CMOS161 was tested after metal1; however, a triple metal version of the 0.35µm process flow is also available.

Table 1, below, outlines the process steps used for the single metal version of the 0.35µm baseline run. The starting material for this process is P-type wafer with <100> orientation and 36-63 Ohm-cm resistivity. The new process utilizes much thinner gate oxide as compared to our previous baseline processes. Lightly doped drain structure, PECVD oxide sidewall spacers, titanium silicide S/D and poly work function engineering was also used in developing the new process. A 0.25µm thick layer of undoped polysilicon material was deposited, then patterned/etched to form the poly gate electrodes. These poly gates were then selectively implanted to have their work function adjusted and matched for desired threshold values, based on the computer simulation results obtained earlier. This was achieved by exposing the N- and P-channel transistors' gate electrode during their respective source/drain implant steps (N S/D and P S/D masks were modified to allow for this). CMP and PECVD TEOS inter-metal dielectric was also used for the triple metal version of the 0.35µm process, which is not shown here. This version is fully supported by our mask set, with additional/more complex circuits to be used on the next run.

Appendix A shows the test chip layout, as described in [8].
Appendix B contains the detailed process flow.

Step 0. Starting wafers Step 1. Initial oxidation Step 2. Zero layer photo Step 3. Pad oxidation/nitride deposition Step 4. N-well photo Step 5. Nitride etch Step 6. N-well implant Step 7. Nitride removal Step 8. Pad oxidation/nitride deposition Step 9. P-well photo Step 10. Nitride etch Step 11. P-well implant Step 12. Nitride removal Step 13. Well drive in Step 14. Pad oxidation/nitride deposition Step 15. Active area photo Step 16. Nitride etch Step 17. P-well field implant photo Step 18. P-well field ion implant Step 19. LOCOS oxidation Step 20. Nitride and pad oxide removal Step 21. Sacrificial oxidation Step 22. Screen oxidation Step 23. NMOS Vt adjust. implant photo Step 24. NMOS Vt adjustment implant	Step 25. PMOS Vt adjust. implant photo Step 26. PMOS Vt adjust. implant Step 27. Gate oxidation, poly-Si dep. Step 28. Gate photo Step 29. Poly Si etch Step 30. P-type LDD implant photo Step 31. P-type LDD implant Step 32. N-type LDD implant photo Step 33. N-type LDD implant Step 34. LDD spacer deposition Step 35. LDD spacer etch Step 36. P+ gate and S/D photo Step 37. P+ gate and S/D implant Step 38. N+ gate and S/D photo Step 39. N+ gate and S/D implant Step 40. Backside etch Step 41. Gate and S/D annealing Step 42. Silicidation Step 43. PSG dep. and densification Step 44. Contact photo Step 45. Contact etch Step 46. Metal 1 deposition Step 47. Metal 1 photo Step 48. Metal 1 aluminum etch Step 49. Sintering Step 50. Testing

Table 1 – Process steps of CMOS161 baseline run

The CMOS161 process included 14 lithography steps. There were masks used on two layers, which brought the total number of masks used down to 9, including a zero layer mask used for printing the ASML alignment marks. The mask set used for the previous six-inch run (CMOS150 run at 1μm technology) was also used for the new six-inch process (CMOS 161) with the exception of layers that required modification. The N+ S/D, P+ S/D masks were modified to allow for in-situ implantation of the udoped polysilicon gate electrodes. The contact mask was scaled down to allow for smaller contacts in the test area of the baseline chip.

The smallest transistor gate length on this design was drawn at 0.4μm, dictated by mask fabrication cost constraints. We are, however, confident that 0.35μm size transistors would have also yielded well, as all the different size transistors down to 0.4 had high yield and were functional. Fig 3 shows top SEM view of the 0.4μm transistor nicely defined by the ASML stepper. Fig 4 presents a section of a ring oscillator with 1μm gates, after poly gate patterning.

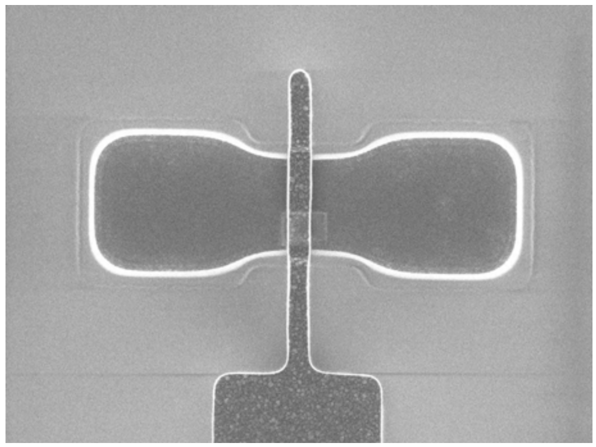


Fig. 3 - Top view SEM image of a 0.4μm transistor after poly gate patterning

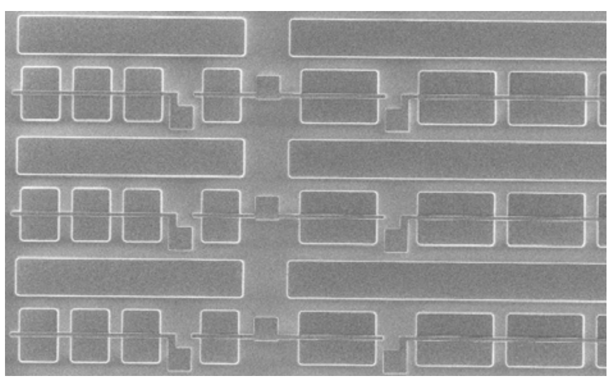


Fig. 4 - Top view SEM image of a 1μm gate ring oscillator section

Table 2 lists all the lithography steps used for the fabrication of CMOS161, as well as the corresponding mask ID and the hard bake methods used for these photolithography steps. All lithography steps were done on a DUV 248nm ASML stepper.

Step	Resist	Mask	Hard bake
Zero layer photo	Shipley UV-210-0.6 9000Å	Zero layer mask	UVBAKE, program J
N-well photo	Shipley UV-210-0.6 9000Å	N-well mask (Dark field)	Oven bake 120C, 2hrs
P-well photo	Shipley UV-210-0.6 9000Å	PFIELD mask (Clear field)	Oven bake 120C, 2hrs
Active area photo	Shipley UV-210-0.6 9000Å	ACTV mask (Clear field)	Oven bake 120C, 2hrs
P-well field imp. photo	Shipley UV-210-0.6 9000Å	PFIELD mask (Clear field)	Oven bake 120C, 2hrs
NMOS Vt adj. implant photo	Shipley UV-210-0.6 9000Å	PFIELD mask (Clear field)	UVBAKE, program J
PMOS Vt adj. implant photo	Shipley UV-210-0.6 9000Å	N-well mask (Dark field)	UVBAKE, program J
Poly gate photo	Shipley UV-210-0.6 9000Å + ARC-600	Poly mask (Clear field)	UVBAKE, program U
P-type LDD implant photo	Shipley UV-210-0.6 9000Å	Mod. P+ S/D mask (Dark filed)	UVBAKE, program J
N-type LDD implant photo	Shipley UV-210-0.6 9000Å	Mod. N+ S/D mask (Dark field)	UVBAKE, program J
P+ Gate & S/D photo	Shipley UV-210-0.6 9000Å	Mod. P+ S/D mask (Dark filed)	UVBAKE, program J
N+ Gate & S/D photo	Shipley UV-210-0.6 9000Å	Mod. N+ S/D mask (Dark field)	UVBAKE, program J
Contact photo	Shipley UV-210-0.6 9000Å + ARC-600	CONT mask (Clear field)	Oven bake 120C, 1hr
Metal1 photo	Shipley UV-210-0.6 9000Å + ARC-600	METAL1 mask (Clear field)	UVBAKE, program U

Table 2 – Lithography steps and related information

The CMOS161 process required 9 ion implantations, all of which were performed at Core Systems (Sunnyvale, Ca). The list of the implantation steps, including implant parameters and blocking materials are shown in Table 3. Implantation splits were used at three different steps of the process, aimed at fine tuning the threshold voltages for both NMOS and PMOS devices. Introduction of a split at the N-well implant step was taken as a precautionary measure to widen the range of the perceptible PMOS threshold voltages. (In Table 3 wafers designated PCH and NCH indicate monitors).

Step	Species	Dose (cm^{-2})	Energy (KeV)	Wafers	Masking materials
N-well implant (Split)	Phosphorus Phosphorus	1E13 2E13	150 150	#1-5, PCH #6-10	180nm Si3N4 600nm PR (Oven bake)
P-well implant	Boron	5E12	60	#1-10, NCH	180nm Si3N4 800nm PR (Oven bake)
P-well field imp.	Boron	2E13	80	#1-10	800nm PR (Oven bake)
NMOS Vt imp. (Split)	BF2 BF2	4E12 6E12	50 50	#1-3,9,10, NCH #4-8	650nm PR (UVBAKE)
PMOS Vt imp. (Split)	Phosphorus Phosphorus	2E12 1E12	30 30	#1-5, PCH #6-10	650nm PR (UVBAKE)
P-type LDD imp.	BF2 BF2	5E13 5E13	10, +7 deg. 10, -7 deg.	#1-10, PCH, Tpoly1	650nm PR (UVBAKE)
N-type LDD imp.	Arsenic Arsenic	5E13 5E13	30, +7 deg. 30, -7 deg.	#1-10, NCH, Tpoly2	650nm PR (UVBAKE)
P+ Gate & S/D im.	Boron	3E15	20	#1-10, PCH, Tploy1	650nm PR (UVBAKE)
N+ Gate & S/D im.	Phosphorus	3E15	40	#1-10, NCH, Tpoly2	650nm PR (UVBAKE)

Table 3 – List of implantation steps and parameters

Table 4 describes the summary of dose splits used for at three ion implantation steps. The computer simulated target groups, includes wafer number 1, 2, 3. The resulting threshold for these implant splits can be followed through by parametric test results shown in Section 5.2.

Table 5 contains the list of tools used during the fabrication of the CMOS161 run.

	NMOS Vt implant 4E12		NMOS Vt implant 6E12	
	PMOS Vt imp. 2E12	PMOS Vt imp. 1E12	PMOS Vt implant 2E12	PMOS Vt implant 1E12
N-WELL implant 1E13	w# 1, 2, 3	-	w# 4, 5	-
N-WELL implant 2E13	-	w# 9, 10	-	w# 6, 7, 8

Table 4 – Ion implantation dose splits

Process module	**Tool***	**Process step**
Lithography	ASML 5500/90 DUV stepper	Listed in Table 2
	SVGCOAT6	
	SVGDEV6	
	UVBAKE	
Plasma etch	AMAT Centura MxP+	Nitride etch
		Oxide etch
		Oxide spacer etch
	Lam 3	Aluminum etch
	Lam 5	Poly-Si etch
High temperature treatment	Tystar 1	Wet/dry oxidation
	Tystar 2	
	Heatpulse 3 (RTP)	Annealing
		Silicidation
CVD	Applied P-5000 (PECVD)	Oxide spacer deposition
	Tystar 9 (LPCVD)	Nitride deposition
	Tystar 10 (LPCVD)	Poly-Si deposition
	Tystar 11 (LPCVD)	PSG deposition
Thin film systems	Novellus	Ti deposition
		Al deposition
	CPA	Al deposition
Wet etch/Cleaning	Sink 6	Pre-furnace piranha clean
		HF dip (10/1, 25/1)
		Rinse (QDR)
	Sink 7	Hot phosphoric etch
		Rinse (QDR)
	Sink 8	Post-lithography piranha clean
		HF dip (5/1)
		Rinse (QDR)

* Detailed tool information at http://microlab.berkeley.edu/labmanual/Labmanualindex.html

Table 5 – Process tool set

4. PROCESS AND DEVICE SIMULATIONS

Process simulator (TSUPREM4) and device simulator (MEDICI) were used to assist the development of the Berkeley Microlab 6 inch, 0.35μm CMOS baseline process. The following table was constructed with reference to the 1997 National Technology Roadmap for Semiconductors (NTRS) for a CMOS 0.35μm process.

	NMOS	PMOS
Vdd	3.3	3.3
Tox	7-8nm	7-8nm
Ioff	0.5-1nA/μm	0.5-1nA/μm
Ion	600μA/μm	280μA/μm

Table 6 – Design specifications for 0.35μm CMOS process

4.1 Process simulation

TSUPREM4 was used to simulate the whole CMOS process. The input deck is given in Appendix C. The simulation structure includes one PMOS and one NMOS transistor. The mask pattern is self-explanatory in the input deck. During the simulation process, the actual fabrication results were fed back and the deck was modified accordingly (e.g. gate oxide thickness was "made-up" to be 8nm as measured by ellipsometry).

The following restrictions were applied during the simulation:

1. Models used for implantation: tr.phosphor, tr.boron, tr.bf2, tr.arsenic.
   Reason: results are more similar to the available data.
2. For diffusion, no damage model had been included (i.e. default FD.FERMI).
   Reason: simulated junction depth with damage model is extraordinarily deep.
3. The simulation is stopped after contact hole opening.

Simulation structure

Figure 5 shows the CMOS structure after contact opening.

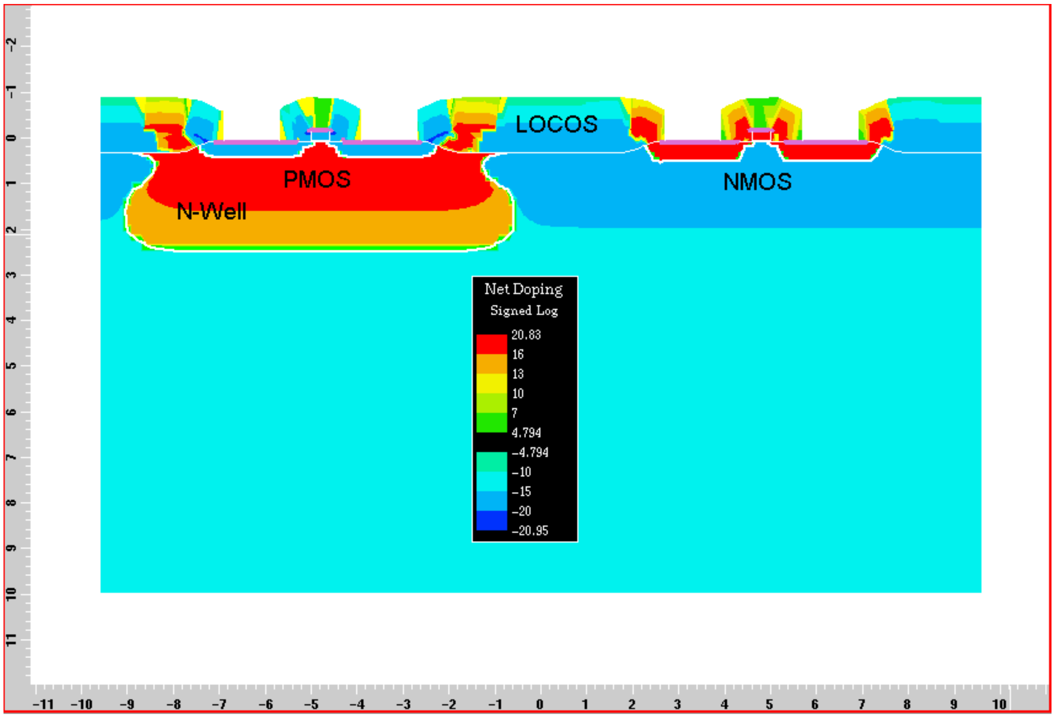


Fig. 5 - Final CMOS structure after process simulation in TSUPREM4

S/D profile (simulation and SRP)

Figure 6 and 7 show the simulated S/D junction profiles of PMOS and NMOS respectively, compared with the Spreading Resistance Profile (SRP) of the actual devices.

It is found that the junction depth of PMOS in simulation is about 80nm deeper than that of SRP. Therefore, the diffusivity of boron is over-estimated in the default model in the simulation. It can be seen that the whole doping profile is shifted by about 80nm. This problem may be corrected by scaling the effective diffusivity of boron in silicon.

For the NMOS case, we can see that the simulation fits very well with the SRP results in the high concentration region (>1E18cm^{-3}) but fails at low concentrations and, as a result, the simulated junction depth is 200nm deeper. One possible explanation is that the Transient Enhanced Diffusion (TED) model in the simulator is again over-estimating the diffusivity of phosphorus. Therefore, the TED has to be re-calibrated in the simulator. It also shows that the simulator gives a shallower silicidation depth (~25nm instead of ~45nm by SRP).

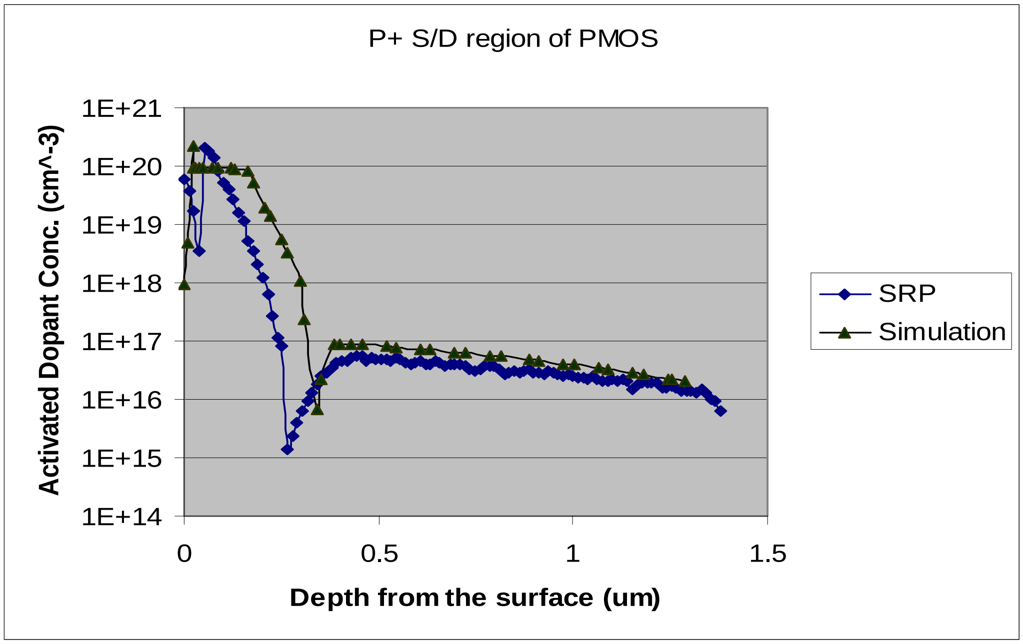


Fig. 6 - Simulated S/D junction profile of PMOS vs. SRP result
The drop at the surface is the region where silicide is formed.

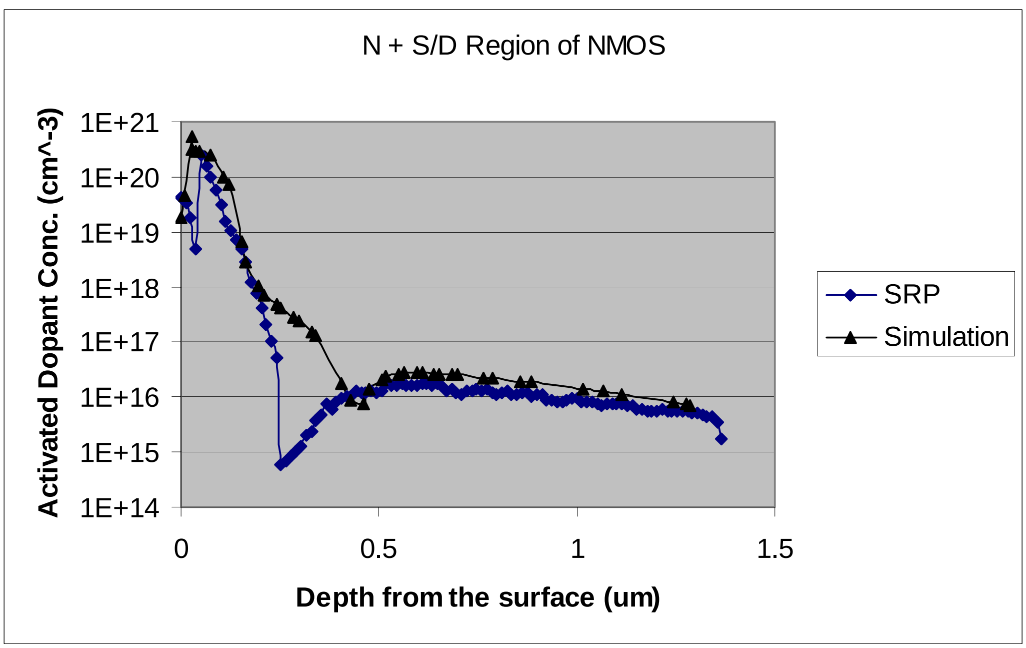


Fig. 7 - Simulated S/D junction profile of NMOS vs. SRP result
The drop at the surface is the region where silicide is formed.

Gate and channel profile (simulation and SRP)

Figure 8 and 9 show the channel dopant profiles of PMOS and NMOS respectively, compared with the Spreading Resistance Profile (SRP) of the actual devices. Since the poly-Si gate was partially polished before SRP, the simulation result is shifted to align with the SRP using the gate oxide. From Figure 8 we can see that the n-well depth is well predicted by the simulation. This agrees with the explanation of n+ S/D junction because the TED effect is not significant in a deep well formation. We can conclude that the diffusion model of phosphorus in silicon fits the reality pretty well except in the TED case.

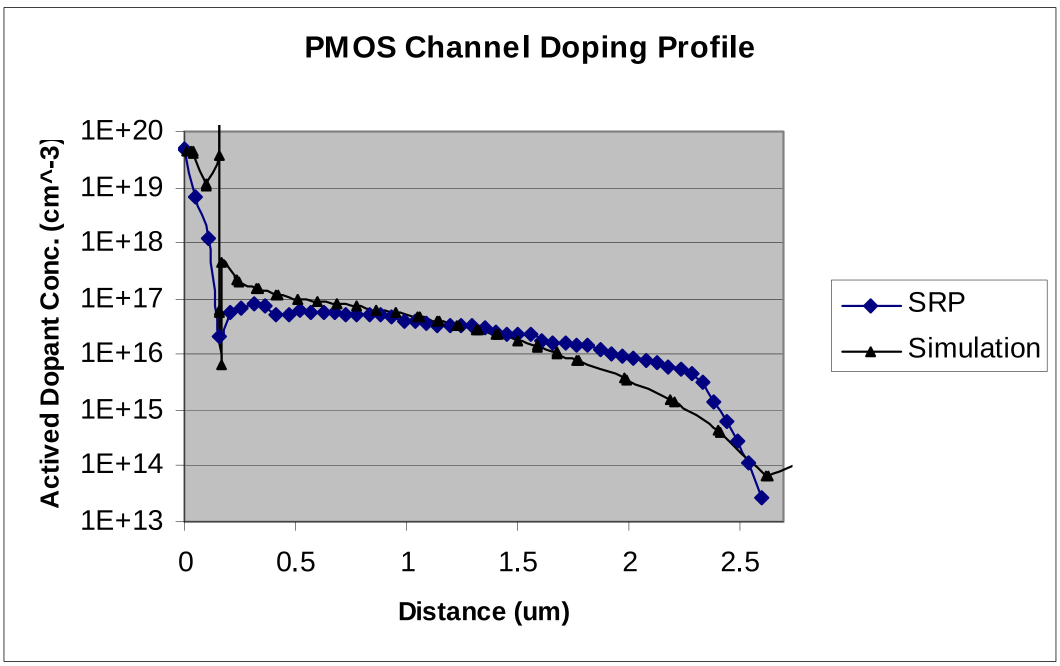


Fig. 8 - Simulated PMOS channel doping profile vs. SRP result
Plot starts with poly-Si gate at 0μm distance.

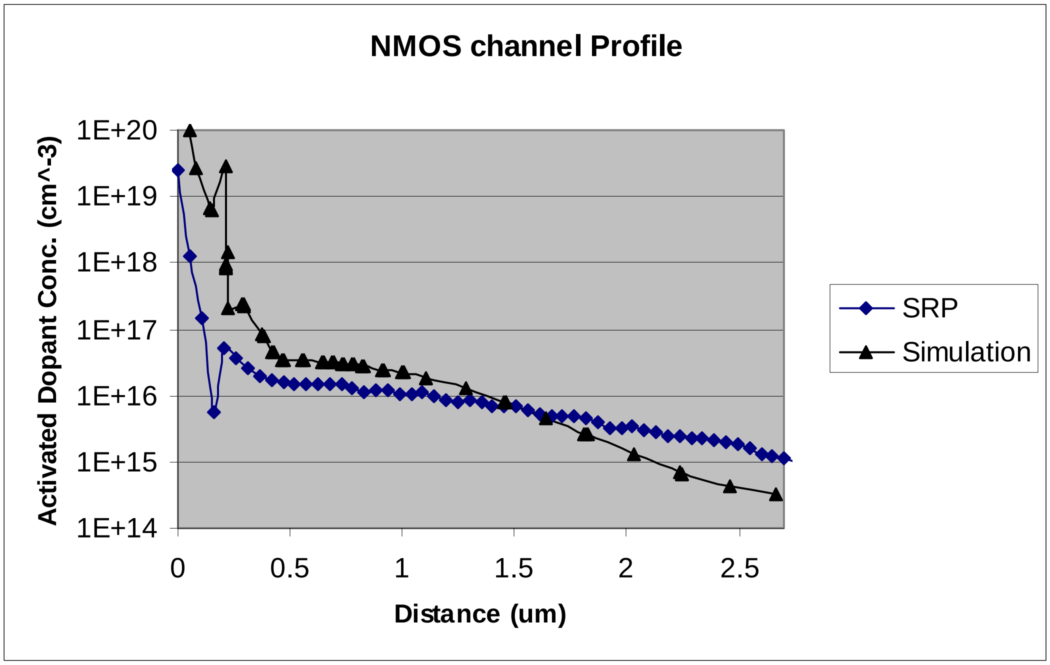


Fig. 9 - Simulated NMOS channel doping profile vs. SRP result
Plot starts with poly-Si gate at 0μm distance.

From Figure 8 and 9, it is found that the activated dopant concentration at the gate electrode/dielectric interface is very low according to the SRP data, compared to the simulations. This is more serious in the NMOS case as shown in Figure 9 (~2 orders of magnitude difference). Therefore, it is expected there will be serious gate depletion in the fabricated device. This indeed can be seen in Figure 10, where the effective capacitance value is about 12% lower in the inversion region than in accumulation. [9]

Figure 10 shows the measured CV curve of a W/L = 100/100 transistor. The fitting curve using the quantum mechanical CV (QMCV) simulator, in which the gate depletion and quantum confinement effects are taken into account, is also included. The fitting parameters of the QMCV simulation are tox = 8nm, gate doping = 2E19, and substrate doping = 2.1E17. In Figure 9, the SRP data shows that the channel concentration (~4E16) is at least five times lower than the value extracted from the CV fitting (2.1E17). On the other hand, the channel concentration obtained from the CV fitting is much closer to the profile simulated by TSUPREM4, shown in Figure 9. Because TSUPREM4 and CV measurements agree for channel concentration, we suspect that the large discrepancy between the SRP and the simulation may be the result of an SRP measurement error. However, this has to be confirmed.

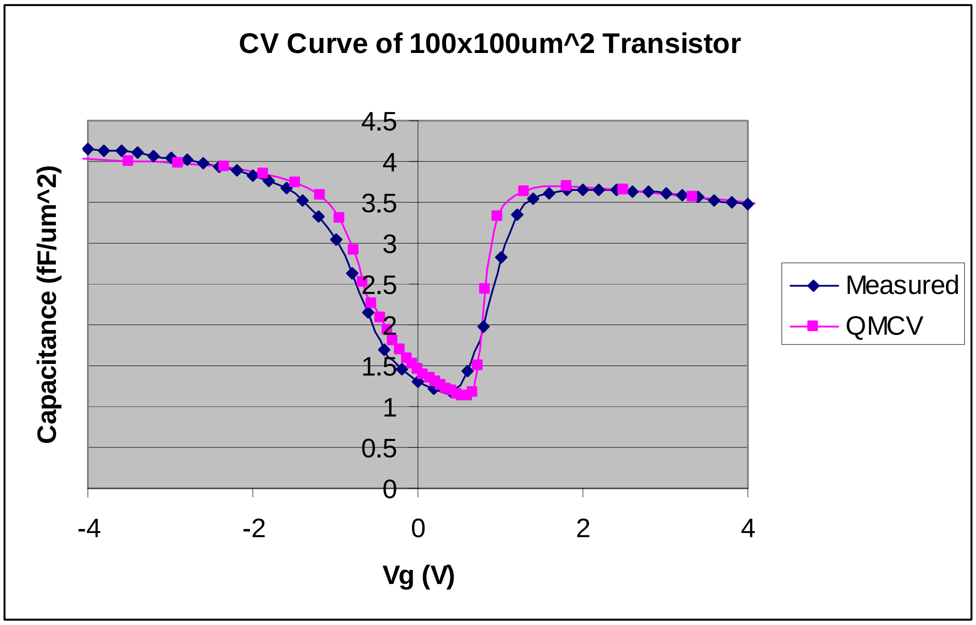


Fig. 10 - Measured and simulated CV curves of NMOS transistor (W/L=100/100)
(Fitting parameters: tox = 8nm, Npoly = 2E19, N-sub = 2.1E17, Vfb = -0.75)

4.2 Device simulation

MEDICI is used for device simulation by using the final structure obtained in TSUPREM4. The input decks are shown in Appendix D. In the simulation, hole and electron equations are solved simultaneously and the band-to-band tunneling (BTBT) and direct tunneling (DT) models were turned on. Interface gate oxide fixed charge is assumed to be 1E10cm^{-2}.

ID-VG

Figure 11 shows the measured and the MEDICI simulated Id-Vg curves of a PMOS transistor with physical gate length = 0.4μm. The simulated and the measured values are reasonably close, only about 70mV difference. There are three main discrepancies between the simulation results and the measurement results. First, the DIBL is higher in the simulation case. A possible reason is that the simulated structure has much deeper S/D junction (Figure 6). Second, there is more GIDL effect for the measured one. This means either the BTBT model is not accurate enough or that some significant traps exist at the region close to the drain. Third, the measured on-current is about 47% lower. The reduction in the on-current may be the result of the gate depletion effect or large S/D resistance.

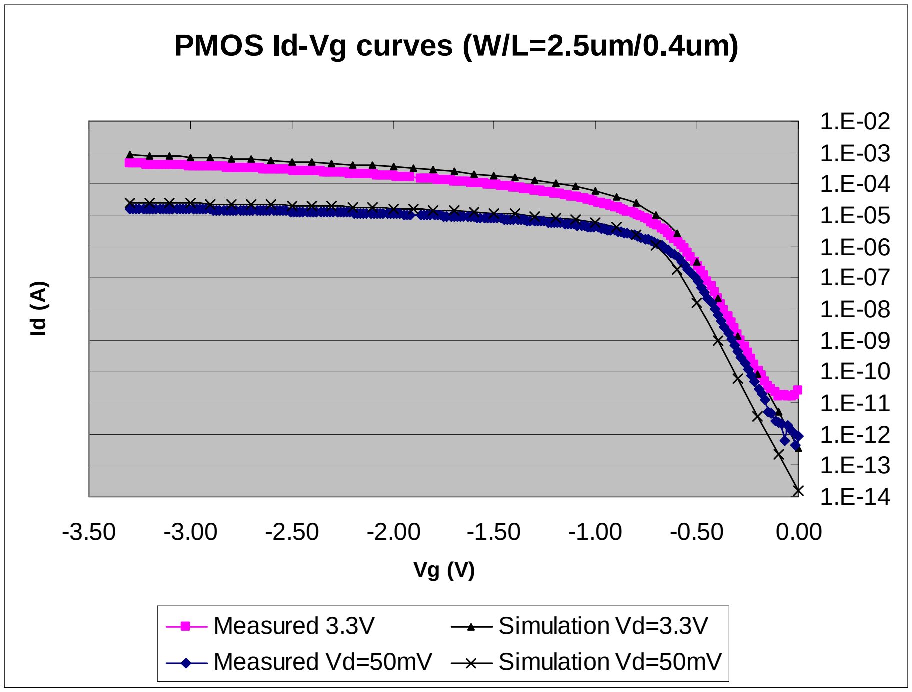


Fig. 11 - Measured and simulated Id-Vg curves of PMOS transistor (W/L=2.5/0.4)

Figure 12 shows the Id-Vg curves of the NMOS transistor with physical gate length = 0.4μm obtained by simulation and also by measurement. There is a big difference between the simulated and measured threshold voltages (about 250mV). One possibility is that the real channel doping is higher than the simulated one. In contradiction, Figure 9 shows that the measured channel doping is lower than the value obtained from the CV measurement. However, as discussed before, there maybe an error in the SRP measurement.

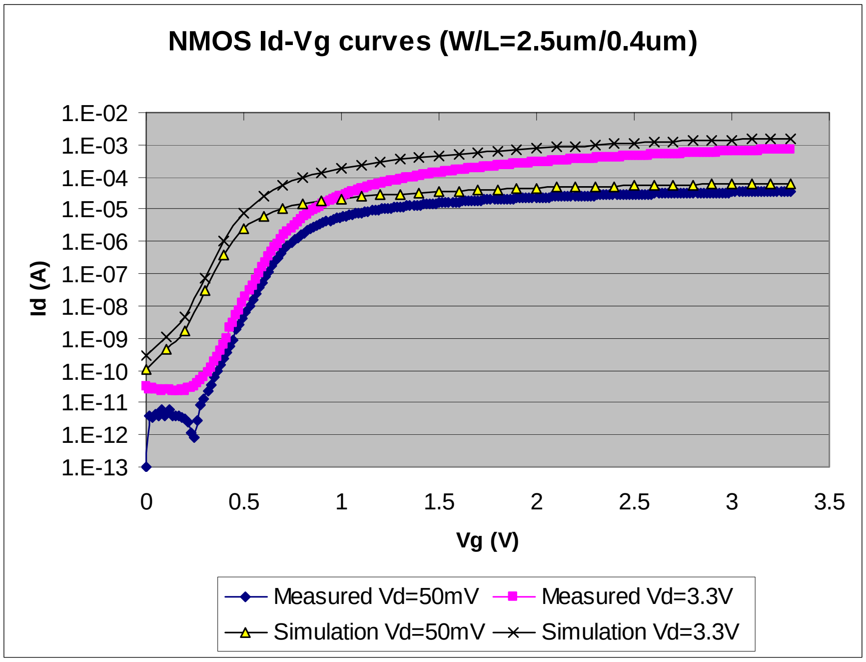


Fig. 12 – Measured and simulated Id-Vg curves of NMOS transistor (W/L=2.5/0.4)

4.3 Simulation conclusions

The process simulation is pretty accurate in predicting the main features of the transistors. However, the following models have to be re-calibrated:

1. Boron Diffusion
2. TED of Phosphorus
3. Enhancement factors of Boron and Phosphorus diffusion coefficients in poly-Silicon

PMOS and NMOS on-current do not meet the specifications (PMOS: 173µA/µm vs. 280µA/µm and NMOS: 287µA/µm vs. 600µA/µm). This can be improved by applying the following:

1. 0.35µm transistor can be fabricated instead of 0.4µm
2. Thermal budget and/or ion implantation energy adjustment to reduce gate depletion effect

However, the leakage current specifications are met well. From the measured results, PMOS Vt can be reduced further by 200mV and NMOS Vt by 330mV while off-current values are still met. With the reduction of the threshold voltage and gate depletion effect, it is expected the requirements in Table 6 can be met eventually. Moreover, thinner gate oxide (>7nm) can be targeted to improve transistor characteristics.

5. MEASUREMENT RESULTS OF THE CMOS161 RUN

5.1 Spreading Resistance Analysis (SRA)

Spreading Resistance Analysis was carried out by Solecon Laboratories Inc. (Reno, NV). Graphical presentation of the measurement results (carrier concentration vs. silicon depth) are shown in Fig 13 and Fig 14, for the channel and source-drain region of transistors, respectively.

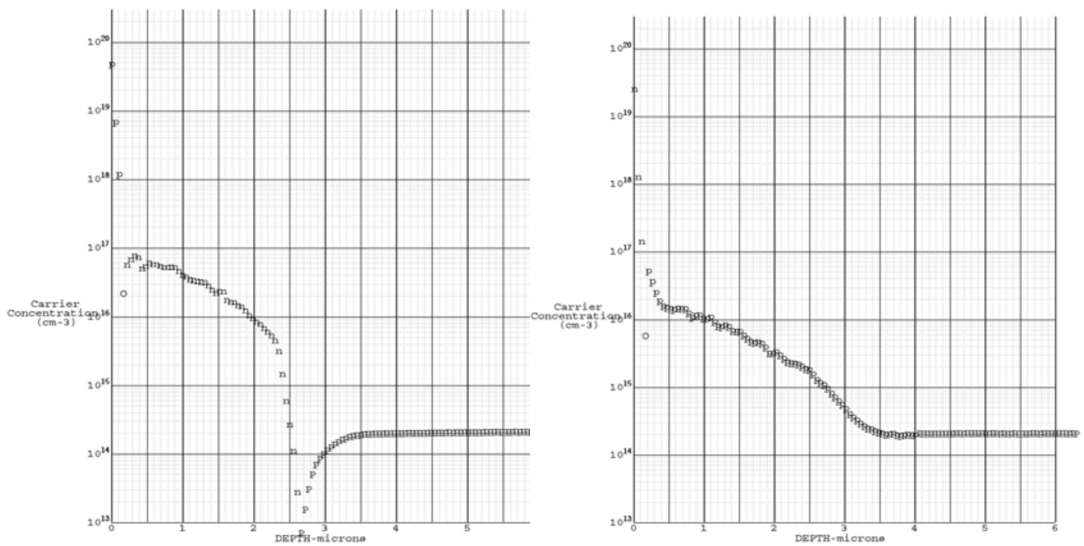


Fig.13 - P-channel (left) and N-channel (right) doping profile under the gate oxide

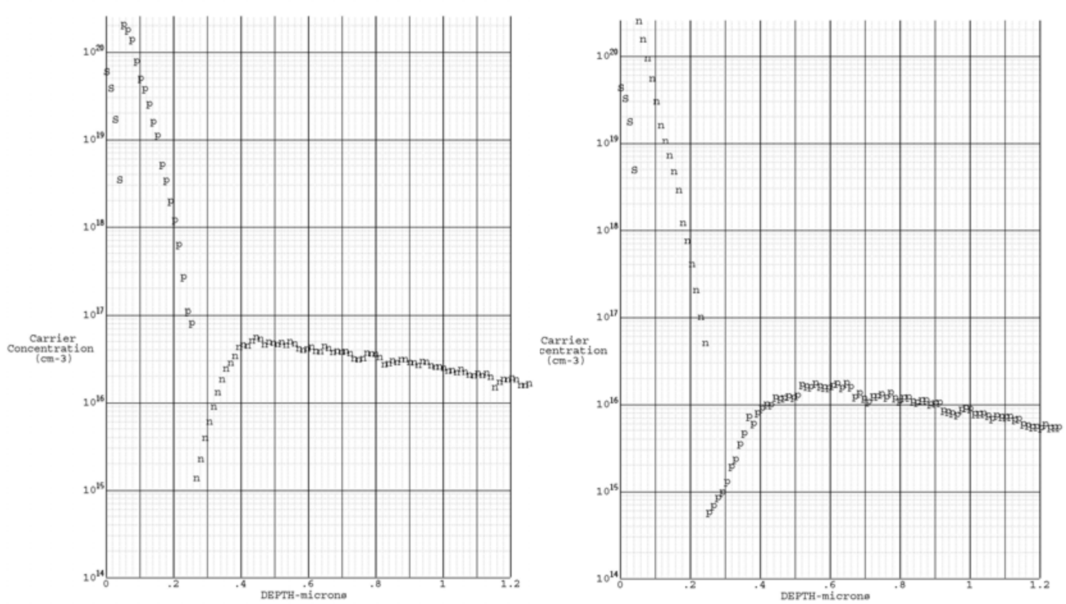


Fig.14 - P+ source-drain (left) and N+ source-drain doping profile

5.2 Electrical measurement results

Electrical measurements were obtained using an automated test system. The HP4062A Semiconductor Parametric Test System utilizes an HP4085A Switching Matrix, an HP4084B Switching Matrix Controller and an Agilent4142B Modular DC Source/Monitor Unit. The system is connected to a Model 2001X Electroglas probe station, which is controlled by a Metrics I/CV software running on a PC workstation. All the test structures and transistors were configured with proper pad array on the chip that would support a 2 x 5 pin probe card (10 tips). Test structure layout was set up this way to allow fast and accurate collection of a large amount of data on device parameters, and other process monitoring related items.

The PC based Metrics software, which includes measurement modules, was used for parametric testing of CMOS161. Test modules in this software were set up/modified based on our old UNIX based Sunbase subroutines, previously used on other baseline runs. The following functions have been used to calculate and display transistor characteristics, and to extract transistor and process parameters:

- IDVD_153 – drain current vs. drain voltage measurement
- VT_153 – drain current vs. gate voltage measurement and threshold voltage calculation
- BODYE – body bias effect calculation
- DIBL_153 – drain induced barrier lowering effect calculation
- SAT_CUR_TRANS – saturation current and trans-conductance calculation
- EFFMOB – effective mobility calculation
- L_SCBR_CONTACT – sheet resistance and contact resistance measurement
- BVds – breakdown voltage of source-drain
- BVox – breakdown voltage of gate oxide

I-V results

The following graphs show typical I-V characteristics of CMOS 161 transistors, which were measured on 0.4µm drawn channel length and 2.5µm width transistors. Fig. 15 and Fig16 demonstrate the Id-Vg, Fig. 17 the Id-Vd curves.

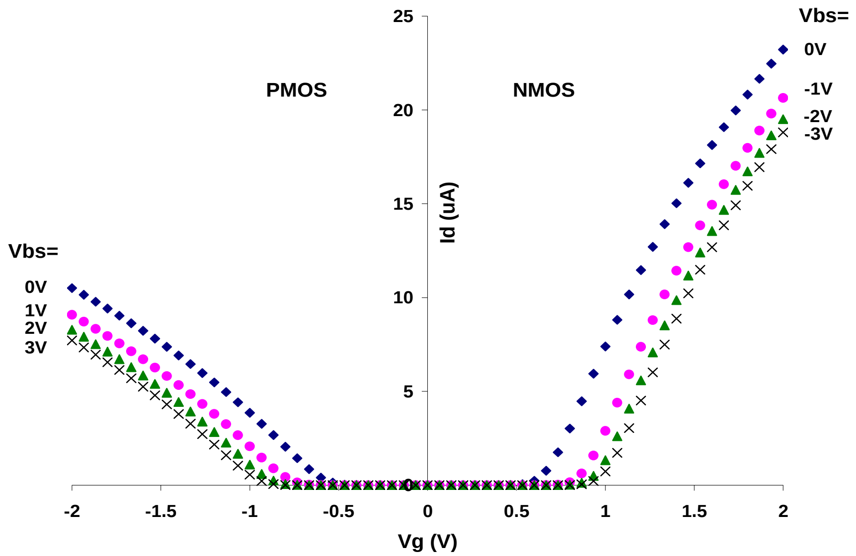


Fig. 15 - Drain current vs. gate voltage at varying substrate bias on PMOS and NMOS transistors in the linear region (Vd=50mV)

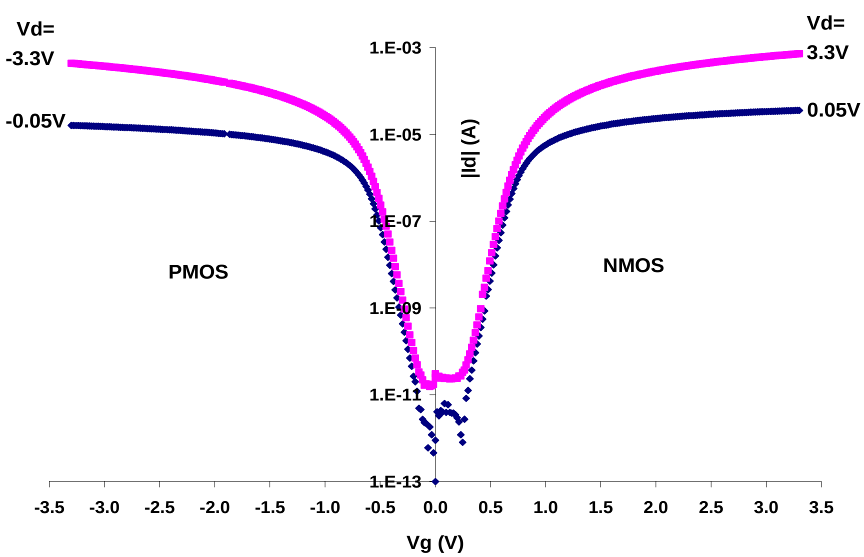


Fig. 16 - PMOS and NMOS sub-threshold characteristics

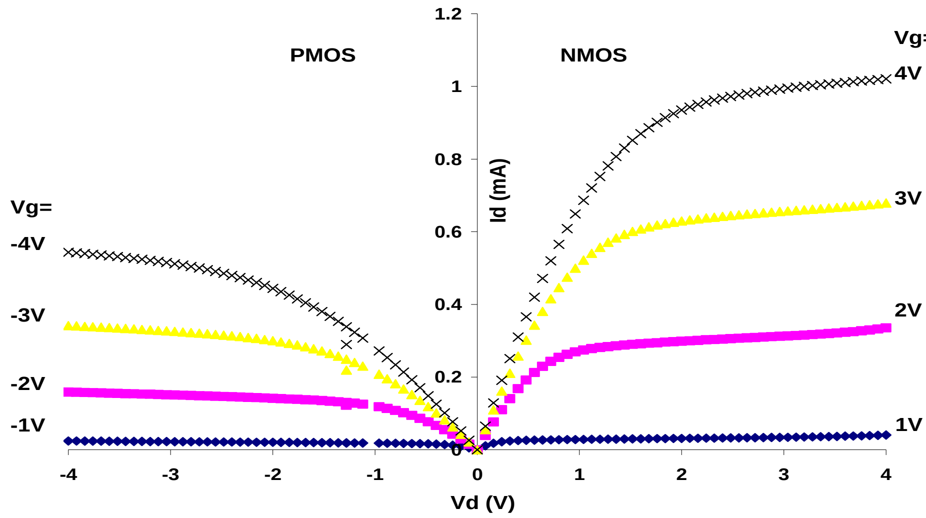
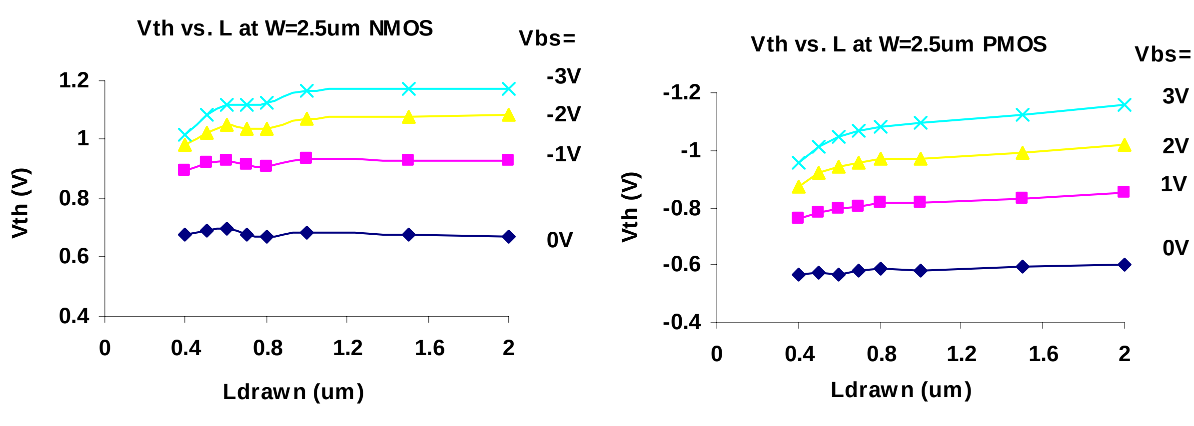


Fig. 17 - Drain current vs. drain voltage characteristics of PMOS and NMOS devices

Threshold voltages of transistors with eight different channel lengths (L=0.4, 0.5, 0.6, 0.7, 0.8, 1.0, 1.5 and 2µm) but the same 2.5µm channel width were plotted on Fig 18. Threshold voltage does not show a large decrease as the channel shortens. The PMOS device under 3V of back bias shows the highest degree of change which is 0.21V between the 0.4µm and the 2µm channel length.



(a) (b)

Fig. 18 - Threshold voltage roll-off vs. drawn channel length at W=2.5µm

Vt implant splits

Threshold voltage adjustment implant splits were applied during the manufacturing process, which was presented previously in Section 3. The following graphs, Fig. 19 and Fig. 20, show how threshold voltages shift as a result of these splits. Each data box is a representation of 185 individual transistor measurements.

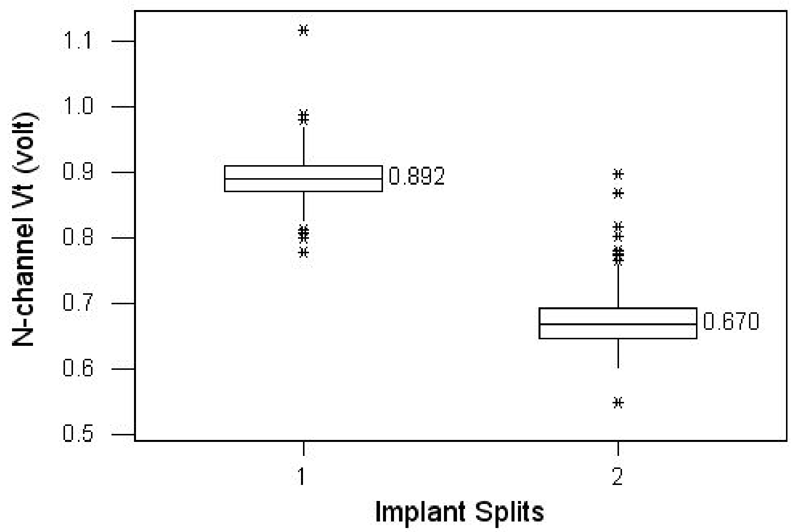


Fig. 19 - Threshold voltages in NMOS split groups:
NMOS split group #1: Wafers #4, 5, 6, 7, 8 (NVt implant dose 6E12)
NMOS split group #2: Wafers #1, 2, 3, 9, 10 (NVt implant dose 4E12)

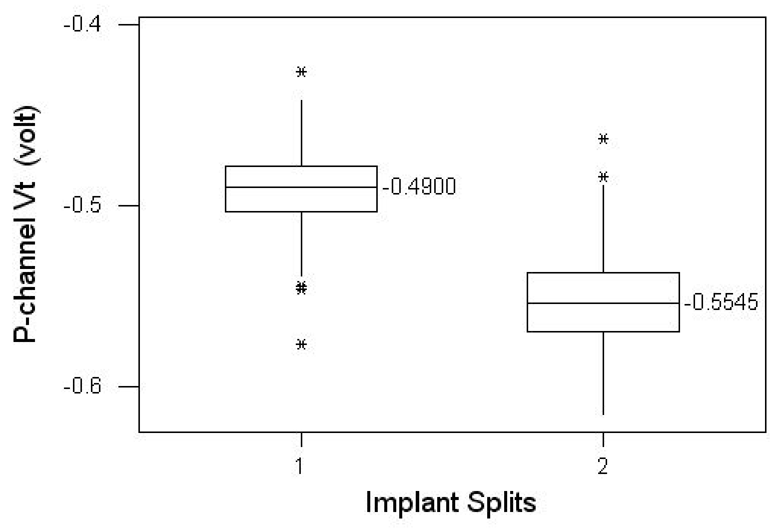


Fig. 20 - Threshold voltages in PMOS split groups:
PMOS split group #1: Wafers #6, 7, 8, 9, 10 (N-Well imp. dose 2E13 and PVt imp. dose 1E12
PMOS split group #2: Wafers #1, 2, 3, 4, 5 (N-Well imp. dose 1E13 and PVt imp. dose 2E12)

Ring oscillators

After the second metal layer deposition ring oscillators were also tested. On the test die we had 1µm and 2µm gate length conventional and 0.6µm and 1.2µm gate length voltage controlled ring oscillators. Each device consists of 31 stages. Metal step coverage limitations in our process caused the 0.6µm oscillators not to function properly. This issue will be addressed in the future version of our 0.35µm process. Measurement results for the 1µm gate length oscillator circuitry are presented in Figure 21, below, displaying a snap shot of the oscilloscope screen, frequency curve and measured values. The average oscillation frequency was measured to be 77.5MHz. The gate delay time using the t_d equation below was calculated to be 0.2 ns.

$$t_d = 1 / 2 * n_s * f_{osc}$$

where n_s is the number of stages (31) and f_{osc} is the oscillation frequency (77.5MHz).

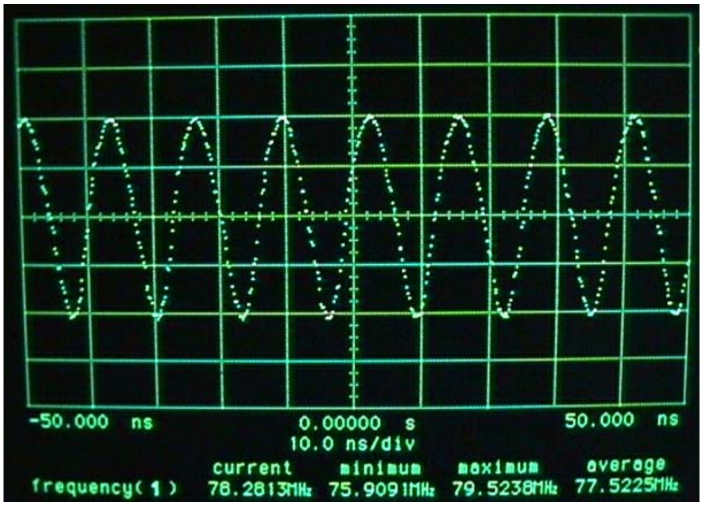
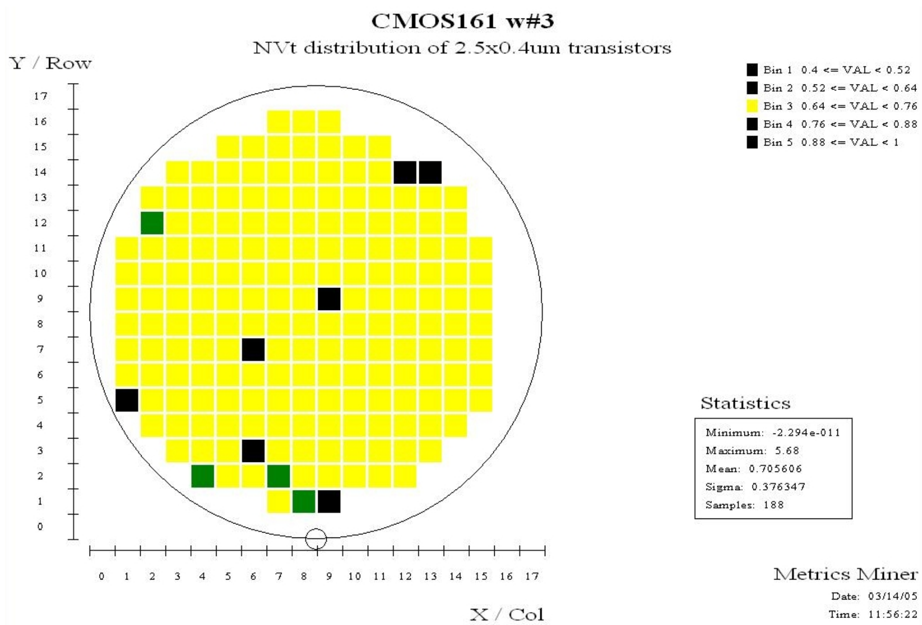


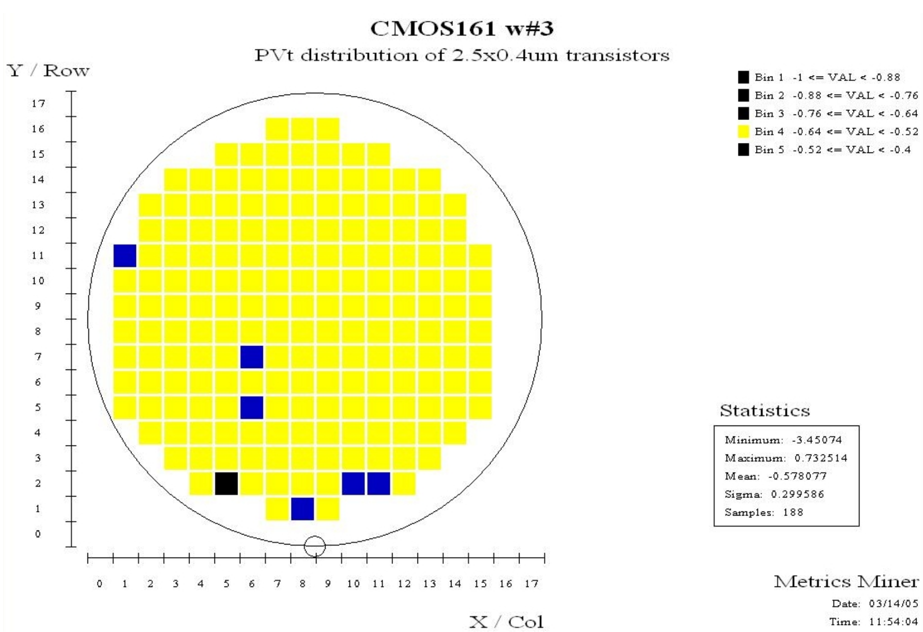
Fig. 21 – Snapshot of the oscilloscope screen showing 1µm gate ring oscillator frequency

Wafer yield data

CMOS161 yielded high above 90%, with working transistors of all sizes. This was a great improvement over all of our previous baseline runs of the 1µm process. Wafer maps of Vt measurements for the 2.5x0.4µm (WxL) NMOS and PMOS transistors are shown on Fig 22. Over 90% of the threshold voltages of the 0.4µm transistors were within the specified voltage range, which are shown in a lighter shade.



a)



b)

Fig. 22 - Wafer map of NVt (a) and PVt (b) distribution on wafer#3 CMOS161

6. SPICE MODEL PARAMETER EXTRACTION FROM BSIMPro+

Parameters extracted by the MOSFET transistor modeling program (BSIMPro+) provide the foundation for circuit simulation tools (SPICE) to perform simulation on a large group of transistors in an integrated circuit [10]. Here we have provided a transistor model summary, specific to the Microlab's 0.35μm technology.

I-V measurements were performed on NMOS and PMOS transistors with 6 different channel lengths (0.4, 0.5, 0.6, 0.7, 0.8 and 1μm) and 2 different channel widths (2.5 and 5μm) to obtain a wide overview of device operational characteristics and meet the requirements of BSIMPro+ simulation. Id-Vg measurements were done in both the linear mode (|Vd|=50mV) and in saturation (Vd=3V), all under four different back-bias conditions (|Vb|=0, 1, 2, 3V); Id-Vd measurements were performed at four different gate voltages (|Vg|=1, 2, 3 and 4V) under two back-bias conditions (|Vb|=0 and 2V). The summary of applied measurement bias conditions is displayed in Table 7, below.

I-V data	Vgs [V]	Vds [V]	Vbs [V]
Ids - Vgs	$0 \le Vgs \le 4$ Vgs step = 0.1	Vds = 0.05 (in linear mode) Vds = 3 (in saturation)	$-4 \le Vbs \le 0$ Vbs steps = 1
Ids – Vds	$1 \le Vgs \le 4$ Vgs step = 1	$0 \le Vds \le 4$ Vds step = 0.1	Vbs = 0 Vbs = -2

Table 7 – I-V measurement bias conditions for NMOS devices
(Voltage polarity is reversed for PMOS)

Wafers were measured on an Electroglas 2001 probe station while I-V data curves were generated by an HP4062A semiconductor parametric test system. More detailed description about the measurement setup can be found in section 5.2 of this report. Test results were then converted into BSIMPro+ data format and provided the basis of the MOSFET modeling.

In Appendix E we show parametric measurement results and BSIMPro+ simulation curves for transistors of the sizes described above this section.

Extracted SPICE parameter sets for NMOS and PMOS are presented in Appendix F.

7. PROCESS AND DEVICE PARAMETERS

Table 8 shows the summary of various measurements and testing results of the CMOS 161 process. Values shown in this table were extracted from measurements on L=0.4μm, W=2.5μm devices.

No.	Parameters	Units	NMOS	PMOS
1	Vt	V	0.67	-0.57
2	Sub Threshold Slope	mV/decade	85	90
3	K (μC_{ox})	$\mu A/V^2$	68	28
4	Delta L	μm	0.048	0.05
5	Delta W	μm	0.058	0.29
6	$\gamma 1$ (|Vsb|=1V)	$V^{1/2}$	0.37	-0.33
7	$\gamma 2$ (|Vsb|=3V)	$V^{1/2}$	0.27	-0.31
8	Surface dopant concentration	Atom/cm3	5.0E+16	6.0E+16
9	Substrate dopant concentration	Atom/cm3	1.0E+16	2.0E+16
10	Tox	nm	8	8
11	Xj (S-D)	μm	0.25	0.26
12	Xw (Well depth)	μm	3.6	2.6
13	Rdiff (sheet resistance)	Ω/square	40	80
14	Rpoly (sheet resistance)	Ω/square	200	200
15	Rwell (sheet resistance)	Ω/square	710	770
16	Rc M1-diff	Ω	79	16
17	Rc M1-poly	Ω	4	0.5
18	| S-D breakdown |	V	>6	>6
19	S-D leakage (Vds=3.3V, Vgs=0V)	pA/μm	12	7.6
20	Eff. Mobility (Vbs=0V, Vgs=1V)	cm^2/V-sec	205	66
21	Ring oscillator frequency (31 stages, 1μm gate, 3.3V)	MHz	77.5	

Table 8 – Process and device parameters of CMOS 161 (W/L=2.5μm /0.4μm)

Methods, measurement conditions and explanations for obtaining the parameters in Table 8 [11]

1. Threshold voltages were measured by the autoprobe Vt module using the linear extrapolation method.

2. Sub-threshold slope values are hand calculated based on the autoprobe DIBLE module (log (Id) vs. Vg). Using the Autoprobe's DIBL module a log (I_d) vs. V_g graph was plotted when the device was operating in the linear region: $V_d = |50mV|$. By picking a decade of Id change on the y scale the corresponding Vg difference was read from the x scale.

3. K values (gain factor in the linear region) were obtained by hand calculation based on the autoprobe Id-Vg measurements when devices were operating in the linear region. Using the Vt module on the Autoprobe, I_d vs. V_g and G_m vs. V_g curves were plotted simultaneously (V_d = |50mV|). The I_d and the corresponding V_g values were picked where Gm maximized. Using the equations

$$K= \mu C_{ox}$$

and

$$I_{ds} = \mu C_{ox} W/L (V_{gs} - V_{th} - V_{ds}/2) V_{ds}$$

values were substituted and K was extracted.

4-5. Effective channel length and width values were obtained from the BSimPro+ simulation program based on the I-V curves measured with the autoprobe Vt and IdVd modules.

6-7. γ_1 and γ_2 (body effect parameters at different body biases) were obtained by hand calculation based on the autoprobe Vt measurements at different body biases. Using the Vt module on the Autoprobe, threshold voltage values were defined under different body bias conditions ($|V_{bs}|$=0V, 1V, 3V). Using

$$V_t = V_{to} + \gamma ((|2\Phi_B|+|Vsb|)^{1/2} - (|2\Phi_B|)^{1/2})$$

and

$$\Phi_B = kT/q \ln (N_{well}/n_i)$$

γ was extracted for $|V_{bs}|$ = 1V, 3V values.

8-9. Surface dopant concentration numbers are based on the SRA results, which matched the values measured on the autoprobe.

10. Gate oxide thickness was measured by the Sopra ellipsometer during processing.

11-12. Well depth and the source-drain depth data arise from the SRA graphs.

13-15. Sheet resistance values were obtained by four-point-probe measurements during processing.

16-17. Contact resistances were measured on designated test structures by the autoprobe CONTR_SCB module.

18. S-D breakdown measurements were taken using the autoprobe.

19. S-D leakage values were calculated based on the graphs given by autoprobe DIBLE module. Using the [log(Id) vs. Vg] graph, the value of I_d was read at $V_g = 0V$ point on the $V_{ds} = 3.3V$ curve.

20. μ_{eff} (effective mobility) data came from autoprobe measurements using the EFFMOB module. Measurement values were modified to reflect actual Cox value. The originally measured value with the Autoprobe's EFFMOB module was multiplied by the factor of 1.23. This ratio was found between the "ideal" Cox value (for t_{ox}=80A) and the lower C_{ox} value that C-V measurement showed in inversion (for "t_{ox}" = t_{ox} + partially depleted poly gate thickness). The factor of 1.23 multiplication was applied because Cox is in the nominator in the μ_{eff} equation

$$\mu_{eff} = g_d / C_{ox} (W/L) (V_g - V_{to})$$

21. Ring oscillator frequency was calculated using the autoprobe RingOsc module.

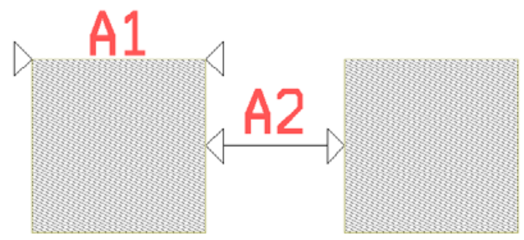
8. LAYOUT DESIGN RULES

The layout design rules shown below were extracted from the working devices of CMOS161. These parameters do not follow any standard design rule methodology, because our periodically implemented modifications focused primarily on gate size reduction. We are, however, confident that with the current toolset in hand further reductions in sizes are possible.

A. P and N Well

A.1 Minimum size: 8.0µm

A.2 Minimum spacing: 1.6µm



B. Active area

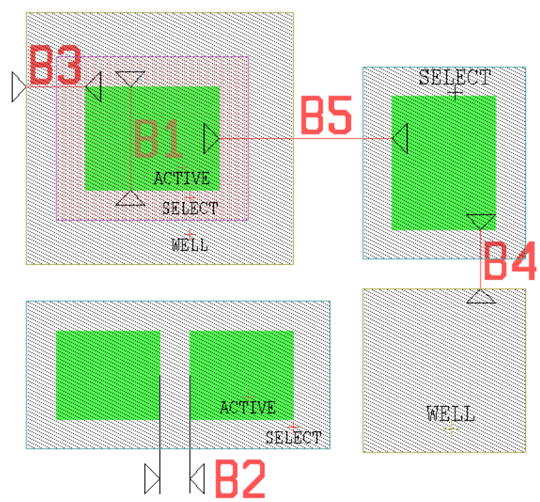
B.1 Minimum size: 2.2µm

B.2 Minimum spacing: 1.5µm

B.3 Space to Well edge: 2.0µm

B.4 Space to Well: 2.6µm

B.5 Space between N+ and P+: 4.6µm



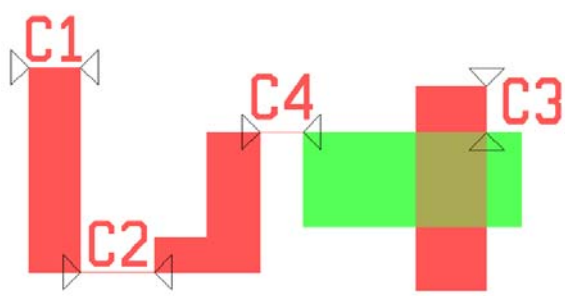
C. Poly

C.1 Minimum size: 0.4µm

C.2 Minimum spacing: 2.2µm

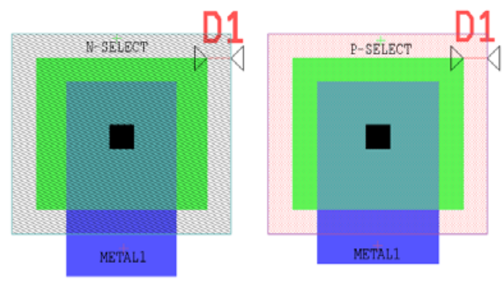
C.3 Gate extension out of Active: 1.4µm

C.4 Minimum spacing to Active: 0.4µm



D. N and P Selects

D.1 Minimum overlap of Active: 0.7µm



E. Active and Poly Contacts

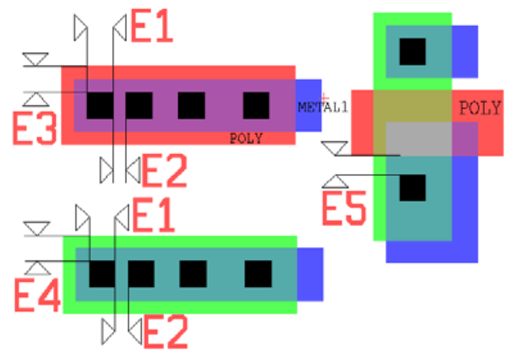
E.1 Minimum size: 1.2µm

E.2 Minimum spacing: 1.4µm

E.3 Minimum overlap by Poly: 0.6µm

E.4 Minimum overlap by Active: 0.8µm

E.5 Minimum spacing to gate: 1.4µm

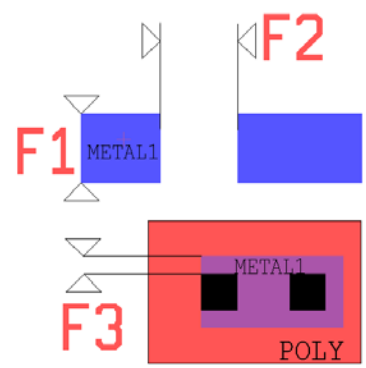


F. Metal 1

F.1 Minimum size: 1.6µm

F.2 Minimum spacing: 1.6µm

F.3 Minimum overlap of Contacts: 0.4µm

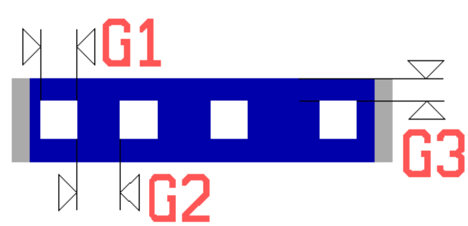


G. Via

G.1 Minimum size: 3.0µm

G.2 Minimum spacing: 4.0µm

G.3 Minimum overlap by Metal1: 2.0µm

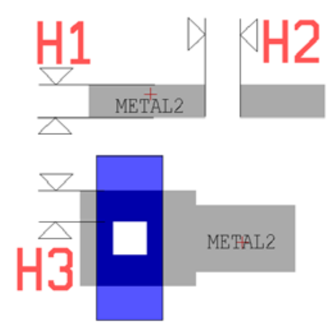


H. Metal 2

H.1 Minimum size: 2.0µm

H.2 Minimum spacing: 2.0µm

H.3 Minimum overlap of Via: 2.0µm



9. FUTURE WORK

In the next version of our 0.35 μm process we would like to improve device "on current", and also to minimize gate depletion effects through better thermal budget engineering. We also hope to improve gate leakage. A better match of P-channel and N-channel transistor Vt will be obtained by adjusting implant dose/energies. We may opt to use a thinner gate oxide for the next generation of the 0.35 μm CMOS baseline process. All of the above are aimed at improving the overall performance of our devices.

The baseline test chip will be revised to utilize the new process better, including more complex circuitry and MEMS devices. We are looking into alternative ways to improve our metal step coverage, which will allow the reduction of contact/via sizes.

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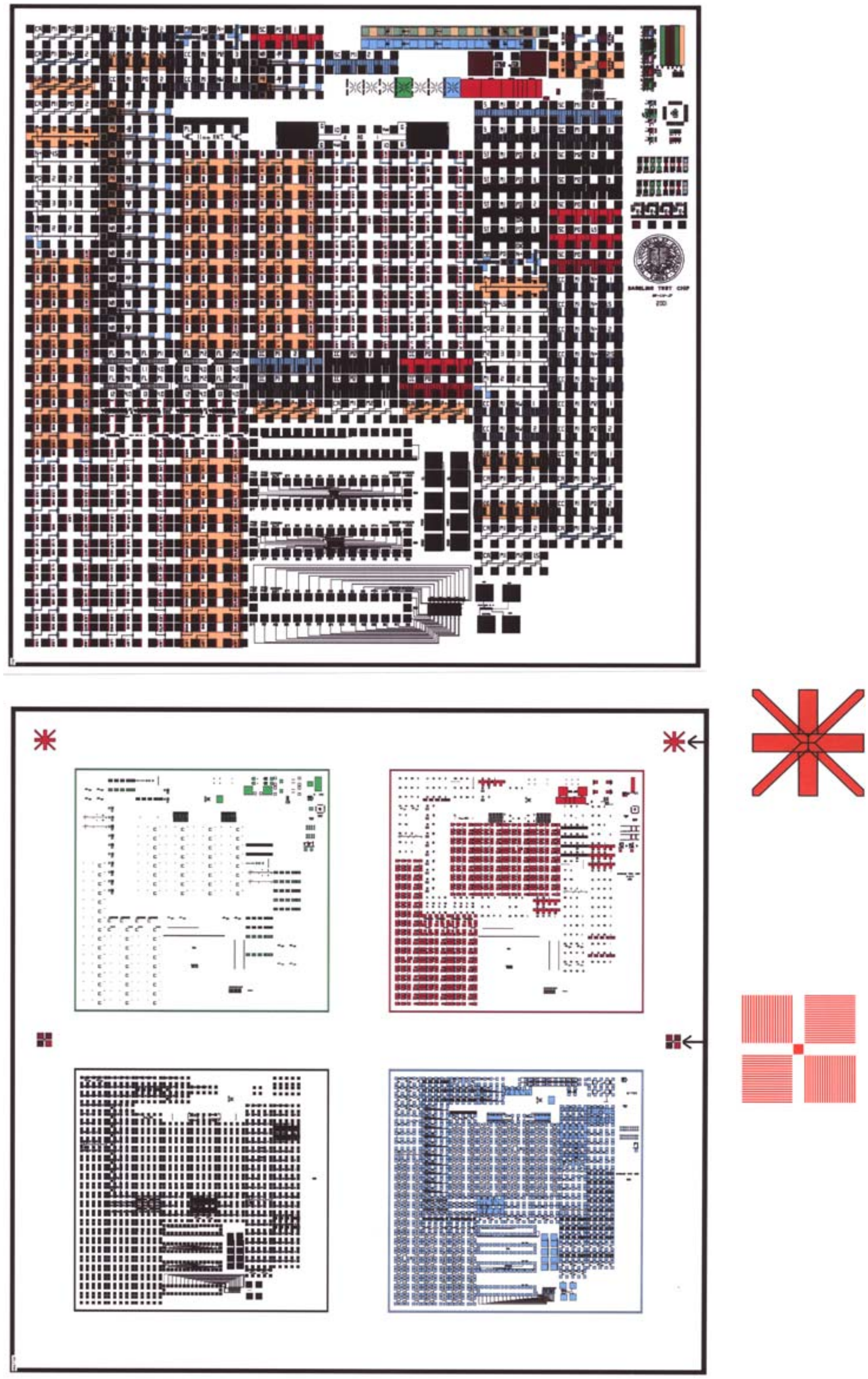
Biographies

Attila Horvath earned his M.S. degree in Electrical Engineering in 2002 from the Technical University of Budapest, Hungary. Since 2002 Attila has been working as a baseline process engineer in the UC Berkeley Microfabrication Laboratory. His main responsibilities are to design, fabricate, test, and evaluate CMOS test devices. He is also actively involved in process related research and development in the Microlab.

Siavash (Sia) Parsa received his M.S. degree in Microelectronics (1988) from Arizona State University. Shortly after graduation, Sia started his career at Integrated Device Technology Inc. (IDT). While working at IDT he held various lead process engineering positions in the photolithography, thin films, ion implantation, process evaluation, and yield enhancement areas, working on SRAM, SMP, logic FIFO and microprocessor products. Sia's last position in the industry was Senior Engineering Manager at Xicor Inc. in Milpitas, California. Sia joined UC Berkeley in 1998, where he has been working as Process Engineering Manager in the Microlab.

Hiu Yung Wong is currently a Ph.D. candidate in the Department of Electrical Engineering and Computer Sciences, in the University of California, Berkeley. He received his B. Eng. and M. Phil. in Computer Science and Engineering from the Chinese University of Hong Kong in 1999 and 2001 respectively. He is interested in the research of Si-based electronic devices, nano-electronics, and integrated circuit design.

Appendix A



Baseline chip layout (top) and four mask layers on one ASML reticle, scaled by ¼ (bottom)
Details in [8]

Appendix B

Microlab CMOS Process

Version 8.1 (2005)

0.35 um, twin-well, 150 mm, double poly-Si, metal

(6" process)

0.0 Starting Wafers (10): 36-63 ohm-cm, p-type, <100>, 6"

1.0 Initial Oxidation: target = 25 (+/- 5%) nm

Include 2 dummies for PM etch characterization.

1.1 TLC clean furnace tube (tystar2)

1.2 Standard clean wafers in sink9 (MOS side):

10/1 HF dip until dewet, spin-dry.

1.3 Dry oxidation at 950 C (2DRYOX):

30 min. dry O2

20 min. dry N2

Measure oxide thickness

2.0 Zero Layer Photo

Standard DUV lithography process:

HMDS (program 1 on svgcoat6), coat (program 2 on svgcoat6),

RPM=1480, UV210-0.6), soft bake (130 C proximity),

Expose (ASML, zero marks mask, 30 mJ/cm2),

PEB (program 1, 130 C on svgdev6) ,

Develop (program 1 on svgdev6).

Hard bake: UVBAKE (program J)

2.1 Etch zero layer into the substrate:

a) Etch oxide in lam2 SIO2MON recipe.

Check actual etch rate, adjust time.

b) Etch silicon in lam4

(target depth=1200 A,) recipe=6000, etch time 30 sec.

Note: Other option lam4 recipe 6200, SF6=25 sec, Cl2=30 sec

(recipe 200 and 6000 merged together)

c) Scribe lot and wafer number on each wafer, including controls.

Ash photoresist in matrix.

d) Measure the depth of the alignment marks using asiq.

3.0 Pad Oxidation/Nitride Deposition:

target = 25 nm SiO2 + 180 nm Si3N4

3.1 TLC clean furnace tube (tystar2). Reserve tystar9.

3.2 Standard clean wafers in sink9

(MEMS and MOS, dip into HF 25:1 until dewet).

Include NCH, PCH control wafers.

3.3 Dry oxidation at 1000 C (2DRYOX):

21 min. dry O2

15 minutes dry N2 anneal.

Measure the oxide thickness on PCH and NCH.

3.4 Deposit 180 nm of Si3N4 immediately (9SNITA):

approx. time = 55 min., temp.= 800 C.

Measure nitride thickness. (nanospec).

4.0 N-Well Photo:

Standard DUV lithography process.

Mask: N-well (dark field)

Standard oven bake (30 min., 120 C)

5.0 Nitride Etch:

Plasma etch nitride in lam4. Recipe: 200

Power:125 W Time:~85 sec. Overetch: no

Selectivity: Si3N4:PR=1:1

Measure Tox on each work wafer. (2 pnts measurement).

Do not remove PR. Inspect.

Measure PR thickness covering active area.tpr >= 700nm

Hard bake again (2 hours, 120 C)

6.0 N-Well Implant: Include PCH.

split: wafers #1-5, PCH: phosphorus, 1E13/cm2, 150 KeV.

wafers #6-10: phosphorus, 2E13/cm2, 150 KeV.

7.0 Nitride removal:

7.1. Remove PR in Matrix. Clean wafers in sink9 MEMS piranha

7.2. Etch nitride in fresh 160 C phosphoric acid in sink7 (~4 hours)

7.3. Etch pad oxide in 5:1 BHF at sink7 until dewet. Include NCH, PCH.

8.0 Pad Oxidation/Nitride Deposition:

Target = 25 nm SiO_2 + 180 nm Si_3N_4

8.1 TLC clean furnace tube (tystar2). Reserve tystar9.

8.2 Standard clean wafers in sink9 (MEMS, MOS, 25:1 HF dip until dewet). Include NCH, PCH.

8.3 Dry oxidation at 1000 C (2DRYOXA):

21 min. dry O_2

15 minutes dry N_2 anneal.

Measure the oxide thickness on NCH and PCH.

8.4 Deposit 180 nm of Si_3N_4 immediately (9SNITA):

Approx. time = 55 min., temp = 800 C.

9.0 P-Well Photo:

Standard DUV lithography process. Mask: PWELL (inverse of NWELL)

Oven bake (30 min., 120 C)

10.0 Nitride Etch:

Plasma etch nitride in lam4. Recipe: 200

Power: 125 W Time:~85 sec. Overetch: no

Selectivity: Si_3N_4:PR=1:1

Measure Tox on each work wafer. (2 pnts measurement).

Do not remove PR. Inspect.

Measure PR thickness covering active area.tpr >= 700nm

Hard bake again (2 hours, 120 C)

11.0 P-Well implant:

Boron, 5E12, 60KeV

Include NCH.

12.0 Nitride removal:

12.1. Remove PR in Matrix. Clean wafers in sink9 MEMS piranha

---

12.2. Etch nitride in fresh 160 C phosphoric acid in sink7 (~4 hours)

12.3. Etch pad oxide in 5:1 BHF at sink7 until dewet. Include NCH, PCH.

13.0 Well Drive-In:

13.1 TLC clean furnace tube (tystar2).

13.2 Standard clean wafers in sink9 (MEMS and MOS).

Include NCH, PCH control wafers.

13.3 Well drive in at 1100 C (2WELLDR):

60 min. temperature ramp from 750 C to 1100 C

150 min. dry O2

15 min. N2

Measure oxide thickness on two wafers.

13.4 Strip oxide in 5:1 BHF until dewet.

Measure Rs on PCH, NCH

14.0 Pad Oxidation/Nitride Deposition:

Target = 25 nm SiO2 + 180 nm Si3N4

14.1 TLC clean furnace tube (tystar2). Reserve tystar9.

14.2 Standard clean wafers in sink9 (MEMS, MOS, 25:1 dip until dewet.) Include NCH, PCH + 2 dummies.

14.3 Dry oxidation at 1000 C (2DRYOXA):

21 min. dry O2

15 minutes dry N2 anneal.

Measure the oxide thickness on NCH.

14.4 Deposit 180 nm of Si3N4 immediately (9SNITA):

Approx. time = 55 min., temp = 800 C.

Only include PCH.

Measure nitride thickness on PCH.

15.0 Active Area Photo:

Std. DUV litho process. Mask ACTV,

Oven bake 120C, 2 hrs.

16.0 Nitride Etch:

Plasma etch nitride in lam4.   Recipe: 200

Power: 125 W   Time:~90 sec.   Overetch: no

Measure Tox on each work wafer (2 points measurement).

17.0 P-Well Field Implant Photo

Std. DUV process. Mask PFIELD (inverse of NWELL+ACT)

Oven bake 120 C, 2hrs.

18.0 P-Well Field Ion Implant

Boron, 2E13, 80KeV

19.0 Locos Oxidation: target = 550 nm

19.1 TLC clean furnace tube (tystar2).

19.2 Remove PR in O2 plasma (matrix).

Standard clean wafers in sink8 MEMS & sink6 MOS piranha,

25:1 HF dip for 5-10 sec.)

Include NCH, PCH.

19.3 Wet oxidation at 1000 C (2WETOXA):

2 hrs. wet O2

20 min. N2 anneal

Measure Tox on 3 work wafers and NCH, PCH.

20.0 Nitride Removal, Pad Oxide Removal.

Include PCH (NCH: no nitride, but LOCOS).

Dip in 10:1 HF for 60 sec to remove thin oxide on top of Si_3N_4.
Etch nitride off in phosphoric acid at 160 C. (sink7) ~3-4 hrs.
Measure pad oxide thickness to verify successful nitride etch.
Etch pad oxide in 5:1 BHF until PCH control wafer dewet.
Etch LOCOS from NCH in 5:1 BHF until dewet.

21.0 Sacrificial oxidation. (Target = 250A)

21.1 TLC clean furnace tube (tystar2).

21.2 Standard clean wafers in sink8 MEMS & sink6 MOS piranha,
25:1 HF dip for 5-10 sec)
Include NCH, PCH.

21.3 Dry oxidation at 900 C (2DRYOXA):
40 min. dry O_2
no N_2 anneal (set to 1 sec)
Measure the oxide thickness on NCH.

22.0 Screen oxidation. Include NCH, PCH

22.1 TLC clean furnace tube (tystar2).

22.2 Standard clean wafers sink6 MOS piranha, dip in 25:1 HF until
NCH, PCH dewet to remove sacr. oxide on active area
(Keep in mind you have LOCOS !)

22.3 Sacrificial Oxide: target = 25 (+/- 2) nm
Dry oxidation at 900 C (2DRYOXA):
40 minutes dry O_2
15 minutes N_2 anneal
Measure Tox on PCH.

23.0 NMOS Vt implant photo
Std. DUV litho. Mask PWELL. UVBAKE (pr. J)

24.0 NMOS Vt implant
Split: BF_2, 4E12, 50KeV, w# 1, 2, 3, 9, 10, NCH.
BF_2, 6E12, 50KeV, W# 4, 5, 6, 7, 8

25.0 PMOS Vt implant photo

Remove PR in matrix, sink8 MEMS piranha clean

Std. DUV litho. Mask NWELL. UVBAKE (pr. J)

26.0 PMOS Vt implant: split: phosphorus, 30 KeV, 2E12/cm2, w#1-5, PCH

phosphorus, 30KeV, 1E12/cm2, w#6-10.

27.0 Gate Oxidation/Poly-Si Deposition:

Target = 8 nm SiO2 + 250 nm undoped poly-Si

27.1 TLC clean furnace tube (tystar1).

Reserve poly-Si deposition tube (tystar10).

27.2 Remove PR in Matrix.

Standard clean wafers sink8 MEMS, sink6 MOS piranha,

25:1 HF dip until dewet on PCH, NCH approx. 2-3 min.

Include Tox (prime P<100>), Tpoly1, Tpoly2 monitoring wafers.

27.3 Dry oxidation in Tystar1 recipe 1THIN-OX

30 min. dry O2 @ 850C

30 min. N2 anneal @ 900 C

Include PCH, NCH, Tox, Tpoly1, Tpoly2 and 3 test dummies.

Note: ALMACK step 25 in furnace process unless the

pre-oxidation furnace temp. is 450C

27.4 Immediately after oxidation deposit 250 nm of undoped

poly-Si (10suplya).

approx. dep. rate= 85 A/min., temp.= 610 C

(Check previous run result)

Include Tpoly1, Tpoly2 and the 3 test dummies.

27.5 Measurements

a) Measure oxide thickness on Tox. (Rudolph and Sopra ell.)

b) Measure Dit and Qox on Tox. (SCA)

c) Measure poly thickness on Tpoly1. (Nanoduv)

d) Stip oxide from NCH, PCH, measure the sheet resisitance.

28.0 Gate Definition:

Standard DUV lithography process.

Mask POLY, Use ARC-600, UVBAKE (U

29.0 Plasma etch poly-Si

29.1 Etch poly in Lam5. Recipe: 5003 with modified over etch step:

Pwr:250 W top, 125W bottom; 200sccm HBr, 5sccm O2,

0sccm He. Selectivity ~60:1 poly to oxide.

Apply ~50% over etch after endpoint in main etch.

29.2 Remove PR (matrix), clean wafers in MEMS piranha.

Measure channel length with CDSEM.

30.0 P-type LDD implant photo

Std. DUV lithography. Mask modified P+S/D. UVBAKE pr. J

31.0 P-type LDD implant. Include PCH, Tpoly1.

BF2, 5e13, 10KeV +7 deg. tilt @ 0 orientation

BF2, 5e13, 10KeV -7 deg. tilt @ 180 orientation

32.0 N-type LDD implant photo

Remove PR in Matrix. Clean wafers in sink8 MEMS piranha.

Std. DUV litho. Mask modified N+S/D. UVBAKE pr. J

33.0 N-type LDD implant. Include NCH, Tpoly2.

As, 5e13, 30KeV +7 deg. tilt @ 0 orientation

As, 5e13, 30KeV -7 deg. tilt @ 180 orientation

34.0 LDD Spacer deposition (spacer width target= 3000 A)

34.1 Remove PR in matrix.

Standard clean wafers (sink8 MEMS, sink6 MOS)

Include 3 dummies.

Reserve and TLC clean tystar2.

34.2 TEOS deposition in P-5000 target=4000-4500 A

Check dep. rate (~ 80 A/min.)

34.3 TEOS annealing 900 C, 30 min. (2HIN2ANA)

34.4 Measure TEOS thickness on active area.

35.0 LDD Spacer Formation

35.1 Plasma etch TEOS in Applied-Centura

Verify actual etch rate (~3000 A/min)

Recipe MXP_OXSP_ETCH_EP

Manual endpoint when signal drops

35.2 Measure spacer with CDSEM.

36.0 P+ Gate & S/D Photo:

Standard DUV Lithography process.

Mask 2nd modified P+ S/D, UVBAKE (“J”)

37.0 P+ Gate & S/D Implant. Include PCH, Tpoly1.

B11, 20 keV, 3E15/cm2

38.0 N+ Gate & S/D Photo:

38.1 Remove PR in Matrix. Std. Clean wafers in sink8 MEMS piranha.

38.2 Standard DUV Lithography process.

Mask 2nd modified N+ S/D, UVBAKE (“J”)

39.0 N+ Gate & S/D Implant. Include NCH and Tpoly2.

Phosphorus, 40 KeV, 3E15/cm2

40.0 Back Side Etch:

40.1 Remove PR in O2 plasma (matrix), piranha clean wafers in

(a) sink8 MEMS side (no dip).

(b) Dehydrate wafers in oven at 120 C for >30 min.

40.2 a) Coat wafers front side, UVBAKE

b) Dip off native oxide in 5:1 BHF in sink8

c) Etch poly-Si in lam5, recipe 5003, no over etch

Etch to endpoint plus 10 sec.

d) Final dip in 5:1 BHF until dewet (~1min)

Incl. NCH, PCH, TPoly1, Tpoly2 to remove native oxide (~20 sec)

41.0 Gate & S/D annealing. Include all test wafers.

41.1 Remove PR in matrix.

41.2 Standard clean wafers in sink8 MEMS and sink6 MOS, no dip

---

41.3 RTA in Heatpulse3, recipe 1050RTA.RCP

900 C, 10 sec., 1050 C, 5 sec in N2

41.4 Check Rs on test wafers: for gate < 250 ohm/sq, for S/D <100.

42.0 Silicide

42.1 Sputter etch in Novellus (ETCHSTD 1 min) or 25:1 HF dip 30 sec

42.2 Sputter 300 Ti in Novellus (Ti300STD). Measure Rs.

42.3 RTA 650 C, 15 sec in N2. Recipe 650RTA6.RCP

42.4 Etch excess Ti/TiN in piranha (120 C, 45 min.) in Sink7.

Measure contact resistance.

43.0 PSG deposition and densification: target 700 nm

43.1 Clean wafers in sink6 MEMS & sink8 MOS side, NO HF dip!

Include PCH and PSG control wafers.

43.2 Deposit 700 nm PSG in tystar11 (11SDLTOA)

Deposition time is approx.: 53 min., 450 C

43.3 Backside etch PSG.

- Coat wafers and UVBAKE pr. J
- Dip into 5:1 BHF until backside dewet
- Matrix PR removal
- Sink8 MEMS & Sink6 MOS piranha clean

43.4 Densify PSG in RTA (heatpulse3). Recipe 900RTA.RCP

900 C, 10 sec, (450 C, 30 sec pre-heat step), silicide chamber.

43.4 Measure PSG thickness on PSG control wafer. Etch (wet) oxide on PCH and measure RS.

44.0 Contact Photo:

Standard DUV lithography process. Use ARC-600.

2nd modified CONT mask. Over-expose contact (30-40 mJ/cm2)

Second PM mark should be exposed, before developing

Oven bake (60 min., 120 C).

45.0 Contact plasma etch in Applied Centura.

Recipe: MXP_OXSP_ETCH_EP

overetch: 15 sec after endpoint signal drops

Measure R with manual probe on Poly and S/D area on each wafer. R~10-100Ohm Check contact holes structure.

46.0 Metallization: target= 600 nm Al

46.1 Remove PR in O2 plasma (Matrix).

46.2 Standard clean wafers in sink8 MEMS no dip, sink6 MOS piranha

Either 25:1/100:1 HF dip 60 sec or Novellus sputter etch to remove native oxide

---

46.3 Sputter Al/2%Si in Novellus:

AL7STD, Measure Rs

47.0 Metal1 Photo:

Standard DUV litho. process, ARC-600.

Mask METAL1. UVBAKE pr. U

48.0 Plasma etch metal1 in lam3.

Standard recipe: approx. time: 1min 25 sec, overetch= 50 %

Check R on Fieldox.

49.0 Sintering

49.1 Remove PR in matrix. Rinse & spin dry at sink8.

49.2 Sinter in Tystar18 H2SINT4A.018 recipe 20 min @ 400 C

50.0 TESTING

Appendix C

Process Simulation Deck for TSUPREM4

```
$ This is modified from version 9
$ updated: 03/20/2005
$ CMOS has been fabricated
$ This deck is for 0.4um transistors
$ hywong2@eecs.berkeley.edu

assign name=step n.val=0

method max.spac=0.05 material=silicon
if (@step<=0)

$Gate to active 2.6um=0.7+1.2+0.7
$Well to active =1um
$boundary to well =1um
$well to well=2um
Line X location=-9.6 spacing =0.1 tag=left
LINE X LOCATION=-5.6 SPACING=0.1
LINE X LOCATION=-4 SPACING=0.1
LINE X LOCATION=0 SPACING=0.1 TAG=MIDDLE
LINE X LOCATION=4 SPACING=0.1
LINE X LOCATION=5.6 SPACING=0.1
Line X location=9.6 spacing =0.1

LINE Y LOCATION=0 SPACING=0.03
LINE Y LOCATION=0.1 SPACING=0.09
LINE Y LOCATION=0.9 SPACING=0.09

$ Substrate required to simulate defects
LINE Y LOCATION=1 SPACING=1
LINE Y LOCATION=10 SPACING=2

else
if.end


if (@step<=1)

INITIALIZE  boron=3e14 <100>
$32-63Ohm-cm

savefile out.file=01.tif tif
else
if.end

if (@step<=2)
$3.0 Pad Oxidation/Nitride Deposition:

loadfile in.file=01.tif tif

$ COMMENT Initial oxidation, 250 A
DIFFUSION temp=1000 time=21 dryO2
DIFFUSION temp=1000 time=15 nitrogen

$nitride deposition
```

```
deposit nitride thick=0.18
Diffusion temp=800 time=55 inert

$ nitride 0.18um
$oxide 280A

$4.0 N-Well Photo:
$NWELL mask
deposit photores positive thick=0.9
etch photo start x=-1 y=-10
etch continue x=-1 y=10
etch continue x=-8.6 y=10
etch done x=-8.6 y=-10
etch nitride trap
implant phosphor energy=150 dose=1e13 impl.tab=tr.phosphor

savefile out.file=02a.tif tif

etch photores
etch nitride
etch oxide
savefile out.file=02.tif tif
else
if.end


if (@step<=3)
$8.0 Pad Oxidation/Nitride Deposition
loadfile in.file=02.tif tif
$ COMMENT Initial oxidation, 250 A
DIFFUSION temp=1000 time=21 dryO2
DIFFUSION temp=1000 time=15 nitrogen

$nitride deposition
deposit nitride thick=0.18
Diffusion temp=800 time=35 inert

$ nitride 0.18um
$oxide 280A

$ 9.0 P-Well Photo:
deposit photores positive thick=0.9
$PFIELD mask
etch photoresist right P1.x=-1 P2.y=10
etch photo left P1.x=-8.6 P2.y=10
etch nitride trap
implant Boron energy=60 dose=5e12 impl.tab=tr.boron

savefile out.file=03a.tif tif

etch photores
etch nitride
Diffusion time=60 temp=750 t.final=1100 inert
diffusion temp=1100 time=150 dryO2
diffusion temp=1100 time=15 nitrogen
etch oxide
savefile out.file=03.tif tif
else
if.end
```

```
if (@step<=4)

loadfile in.file=03.tif tif
$14.0 Pad Oxidation/Nitride Deposition

$ Pad oxide, nitride formation

DIFFUSION temp=1000 time=21 dryO2
DIFFUSION temp=1000 time=15 nitrogen
deposit nitride thick=0.18
$ Target 0.18 measured 0.22um
$Still use 0.18
Diffusion temp=800 time=55 inert

$ Oxide=264A measured 300A
savefile out.file=04.tif tif
else
if.end

if (@step<=5)
$ 15.0 Active Area Photo:

loadfile in.file=04.tif tif
$Active Area Definition
deposit photores positive thick=0.9
etch left photores p1.x=-7.6 p2.x=-7.6
etch right photores p1.x=7.6 p2.x=7.6
etch photo start x=2.05 y=-10
etch continue x=2.05 y=10
etch continue x=-2.05 y=10
etch done x=-2.05 y=-10
etch nitride trap
etch photoresist
savefile out.file=05.tif tif
else
if.end

if (@step<=6)

loadfile in.file=05.tif tif

$field implant
$ FIELD implantation mask
$ 17.0 P-Well Field Implant Photo (inverse of NWELL+ACT)
deposit photores positive thick=0.9
etch left photores p1.x=-8.6 p2.x=-8.6
etch right photores p1.x=7.6 p2.x=7.6
etch photo start x=2.05 y=-10
etch continue x=2.05 y=10
etch continue x=-1.05 y=10
etch done x=-1.05 y=-10
implant Boron energy=80 dose=2e13 impl.tab=tr.boron
etch photoresist
savefile out.file=06.tif tif
else
if.end

if (@step<=7)
$19.0 Locos Oxidation:  target = 550 nm
loadfile in.file=06.tif tif
```

```
$ COMMENT Field Oxidation, 4000 +/- 400 A
DIFFUSION temp=1000 time=120 wetO2
DIFFUSION temp=1000 time=20 INERT
Etch nitride

$oxide thickness: measured 5200, simulated 6000
savefile out.file=07.tif tif
else
if.end

if (@step<=8)
$22.0 Screen oxidation. Include NCH, PCH

loadfile in.file=07.tif tif
$etch pad oxide
ETCH oxide thick=0.026
$ COMMENT sacrificial oxide, 250 A
DIFFUSION temp=900 time=40 dryo2
ETCH oxide thick=0.0320
$ COMMENT screening oxide, 250 A
DIFFUSION temp=900 time=40 dryo2
DIFFUSION temp=900 time=15 INERT
$simulated 130A measured 200A
deposit  oxide thick=0.006
$ COMMENT PVT Implant boron to shift the threshold
$NWELL mask
deposit photores positive thick=0.9
etch photo start x=-1 y=-10
etch continue x=-1 y=10
etch continue x=-8.6 y=10
etch done x=-8.6 y=-10
IMPLANT phosphor dose=2E12 energy=30 impl.tab=tr.phosphor
etch photoresis

deposit photores positive thick=0.9
$PWELL mask
etch photo start x=1 y=-10
etch continue x=1 y=10
etch continue x=8.6 y=10
etch done x=8.6 y=-10
IMPLANT BF2 dose=4E12 energy=50 impl.tab=tr.BF2
etch photoresis
savefile out.file=08.tif tif
else
if.end

if (@step<=9)

loadfile in.file=08.tif tif
etch oxide thick=0.021
$ COMMENT Oxidize the gate with dry/wet/dry 70 +/- 15 A

DIFFUSION temp=850 time=30 dryo2

$simulated 67A, real 80A
deposit  oxide thick=0.0014
$for compensation
$ COMMENT Deposit poly gate 2500 +/- 300 A
diffusion temp=900 time=30 Nitrogen
```

```
DEPOSIT polysilicon thickness=.25 temp=610
DIFFUSION temp=610 time=30 inert

savefile out.file=09.tif tif
else
if.end

if (@step<=10)
$28.0 Gate Definition:

loadfile in.file=09.tif tif
$ poly etching
deposit photoresis thick=0.9
ETCH photo LEFT P1.X=-5
ETCH photo right P1.X=5
etch photo start x=4.6 y=-10
etch continue x=4.6 y=10
etch continue x=-4.6 y=10
etch done x=-4.6 y=-10
etch poly trap
etch photo
savefile out.file=10.tif tif
else
if.end

if (@step<=11)
loadfile in.file=10.tif tif
deposit photo thick=0.9
etch photo start x=-2 y=-10
etch continue x=-2 y=10
etch continue x=-7.6 y=10
etch done x=-7.6 y=-10
$ P+S/D mask
implant BF2 energy=10 dose=5e13 tilt=7 impl.tab=tr.bf2
implant BF2 energy=10 dose=5e13 tilt=-7 impl.tab=tr.bf2
etch photo
savefile out.file=11.tif tif
else
if.end

if (@step<=12)
loadfile in.file=11.tif tif
deposit photo thick=0.9
etch photo start x=2 y=-10
etch continue x=2 y=10
etch continue x=7.6 y=10
etch done x=7.6 y=-10
$ N+S/D mask
implant arsenic energy=30 tilt=7 dose=5e13 impl.tab=tr.arsenic
implant arsenic energy=30 tilt=-7 dose=5e13 impl.tab=tr.arsenic
etch photo
savefile out.file=12.tif tif
else
if.end

if (@step<=13)
$ 34.0 LDD Spacer deposition (spacer width target= 3000 A)

loadfile in.file=12.tif tif
deposit oxide thick=0.30
```

```
diffusion temp=450 time=24 inert
diffusion temp=900 time=30 inert
etch oxide trap thick=0.30
savefile out.file=13.tif tif
else
if.end

if (@step<=14)
loadfile in.file=13.tif tif
deposit photo thick=0.9
etch photo start x=-2 y=-10
etch continue x=-2 y=10
etch continue x=-7.6 y=10
etch done x=-7.6 y=-10
$ P+S/D mask
$ 36.0 P+ Gate & S/D Photo:
implant boron energy=20 dose=3e15 impl.tab=tr.boron
etch photo
savefile out.file=14.tif tif
else
if.end

if (@step<=15)
loadfile in.file=14.tif tif
deposit photo thick=0.9
etch photo start x=2 y=-10
etch continue x=2 y=10
etch continue x=7.6 y=10
etch done x=7.6 y=-10
$ N+S/D mask
implant phosphor energy=40 dose=3e15 impl.tab=tr.phosphor
etch photo
$annealing
diffusion temp=900 time=0.167
diffusion temp=1050 time=0.083

savefile out.file=15.tif tif
else
if.end

if (@step<=16)
loadfile in.file=15.tif tif
etch oxide trap thick=0.010
deposit mat=titanium thick=0.030
diffusion time=0.25 temp=650 inert
etch mat=titanium all

savefile out.file=16.tif tif
else
if.end

if (@step<=17)
$PSG deposition and densification
loadfile in.file=16.tif tif
deposit oxide thick=0.7
diffusion temp=450 time=53 inert
diffusion temp=900 time=0.167 inert
savefile out.file=17.tif tif
else
if.end
```

```
if (@step<=18)
loadfile in.file=17.tif tif
deposit photoresist thick=0.9
etch photoresist start x=-6.9 y=-10
etch photoresist continue x=-6.9 y=10.0
etch photoresist continue x=-5.7 y=10.0
etch photoresist done x=-5.7 y=-10
etch photoresist start x=6.9 y=-10
etch photoresist continue x=6.9 y=10.0
etch photoresist continue x=5.7 y=10.0
etch photoresist done x=5.7 y=-10
etch photoresist start x=-3.9 y=-10
etch photoresist continue x=-3.9 y=10.0
etch photoresist continue x=-2.7 y=10.0
etch photoresist done x=-2.7 y=-10
etch photoresist start x=3.9 y=-10
etch photoresist continue x=3.9 y=10.0
etch photoresist continue x=2.7 y=10.0
etch photoresist done x=2.7 y=-10
etch oxide trap
etch photoresist
savefile out.file=18.tif tif

else
if.end

if (@step<=19)
loadfile in.file=18.tif tif
savefile out.file=19.tif tif
else
if.end

if (@step<=20)
loadfile in.file=19.tif tif

STRUCTUR truncate bottom y=1.4
$NMOS
$STRUCTUR truncate left x=1
$savefile        outf=nmos.tif   tif
$PMOS
STRUCTUR truncate right x=-2
STRUCTUR truncate left x=-8
savefile        outf=pmos.tif   tif

$PLOT.2D

$electrode x=3 y=0.13 name=source
$electrode x=4.8 y=-0.13 name=gate
$electrode x=6 y=0.13 name =drain
$savefile out.file=nmos.med MEDICI

electrode x=-3 y=0.13 name=source
electrode x=-4.8 y=-0.13 name=gate
electrode x=-6 y=0.13 name =drain
savefile out.file=pmos.med MEDICI

else
if.end
```

Appendix D

Process Simulation Deck for MEDICI

NMOS:

```
$ Medici 0.4 micron n-channel MOSFET

mesh        inf=./nmos.med    tsuprem4 elec.bot=0 poly.ele=0

electrode   name=substrate    y.min=1.2

contact           name=gate   neutral
contact           name=substrate neutral
contact           name=source neutral
contact           name=drain neutral

model       conmob            hpmob       consrh      auger
+btbt
+bt.model=1 bt.local=0 bt.quad

$regrid on doping
REGRID doping log ratio=2 smooth=1 ignore=2

$save
savefile    out.file=afterregridnmos.tif  tif
symb        carrier=2 newton
solve       v(drain)=0 v(gate)=0 v(source)=0 v(substrate)=0
+out.file=biasing.tif tif all

interfac QF=1E10


solve

save out.file=init.sol

save mesh out.file=nmos.msh w.models
solve       v(drain)=0.05     vstep=0.0   nstep=1           electrode=drain
log         ivfile=nmos05.log
symb        carrier=2   newton
solve       v(gate)=0 v(drain)=0.05 vstep=0.1 nsteps=33 electrode=gate
+v(source)=0 v(substrate)=0
log   ivfile=temp.log
solve       v(drain)=0.05     vstep=0.0   nstep=1           electrode=drain

solve       v(gate)=0 v(drain)=0.5  electrode=gate
+v(source)=0 v(substrate)=0
solve       v(gate)=0 v(drain)=1.0  electrode=gate
+v(source)=0 v(substrate)=0
solve       v(gate)=0 v(drain)=2.0  electrode=gate
+v(source)=0 v(substrate)=0
solve       v(gate)=0 v(drain)=3.0  electrode=gate
+v(source)=0 v(substrate)=0
solve       v(gate)=0 v(drain)=3.3  electrode=gate
+v(source)=0 v(substrate)=0
log         ivfile=nmos.log
symb        carrier=2   newton
```

```
solve       v(gate)=0 v(drain)=3.30 vstep=0.1 nsteps=33 electrode=gate
+v(source)=0 v(substrate)=0
```

PMOS:

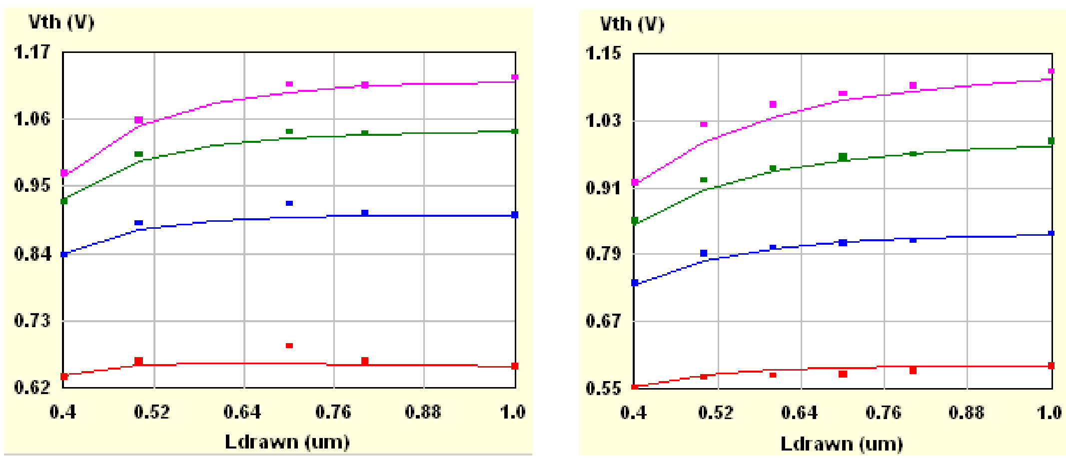
```
$ Medici 0.4 micron P-channel MOSFET

mesh        inf=./pmos.med    tsuprem4 poly.ele=0

electrode   name=substrate    y.min=1.4
contact           name=gate   neutral
contact           name=substrate neutral
contact           name=source neutral
contact           name=drain neutral

model       conmob            hpmob       consrh      auger print
+btbt bt.model=3 bt.local=0 bt.quad

$regrid on doping
REGRID doping log ratio=2 smooth=1 ignore=2

$save
interfac QF=1E10
savefile    out.file=afterregridnmos.tif  tif
symb        carrier=2
$solve            v(drain)=3.3 v(gate)=0 v(source)=0 v(substrate)=0
$+out.file=biasingp.tif tif all



symb        carrier=2   newton
solve initial
save out.file=init.sol
save mesh out.file=pmos.msh w.models
solve       v(drain)=0.05     vstep=0.0   nstep=1           electrode=drain
log         ivfile=pmos05.log
symb        carrier=2   newton
solve       v(gate)=0 v(drain)=-0.05      vstep=-0.1 nsteps=33 electrode=gate
+v(source)=0 v(substrate)=0
log   ivfile=temp.log
solve       v(gate)=0 v(drain)=-1.0 electrode=gate
+v(source)=0 v(substrate)=0
solve       v(gate)=0 v(drain)=-2.0 electrode=gate
+v(source)=0 v(substrate)=0
solve       v(gate)=0 v(drain)=-3.0 electrode=gate
+v(source)=0 v(substrate)=0
log         ivfile=pmos33.log
symb        carrier=2   newton
solve       v(gate)=0 v(drain)=-3.3 vstep=-0.1 nsteps=33 electrode=gate
+v(source)=0 v(substrate)=0
```

Appendix E

BSIMPro+ simulation results

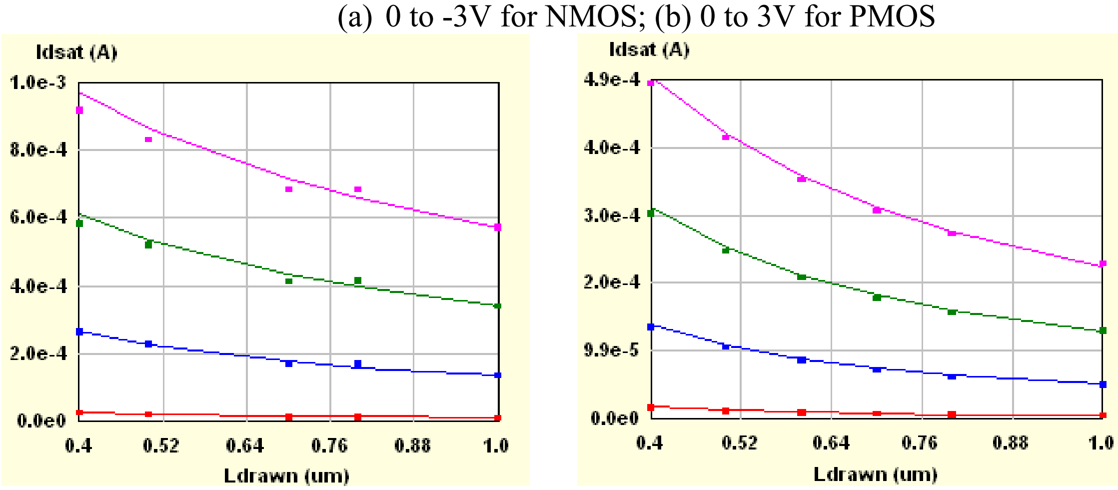
Using the BSIMPro+ MOSFET modeling tool we were able to create a general transistor model based on our measurement results for both NMOS and PMOS devices that provide a very good fit for all the studied transistors with the investigated gate length and width. In the following figures (Fig. 23 – 38), we demonstrate the parametric measurement results and the BSIMPro+ simulation curves displayed on top of each other. Dotted lines represent the measurement data points, while the continuous curves show the simulation results. Six graphs are plotted for each transistor size describing

(a) Id–Vgs at |Vds|=50mV for |Vbs|=0 to 3V
(b) Id-Vds at Vbs=0v for |Vgs|=1 to 4V
(c) Id–Vgs at |Vds|=50mV for |Vbs|=0 to 3V; plotting Id on logarithmic scale
(d) Gds-Vds at Vbs=0V for |Vgs|=1 to 4V
(e) Gm-Vgs at |Vds|=50mV for |Vbs|=0 to 3V
(f) Rout-Vds at Vbs=0V for |Vgs|=1 to 4V.



(a) (b)

Fig. 23 - Threshold voltage vs. drawn channel length at W=2.5μm with substrate bias
(a) 0 to -3V for NMOS; (b) 0 to 3V for PMOS



(a) (b)

Fig. 24 - Saturation current vs. channel length at Vbs=0V with gate bias
(a) 1 to 4V for NMOS; (b) -1 to -4V for PMOS

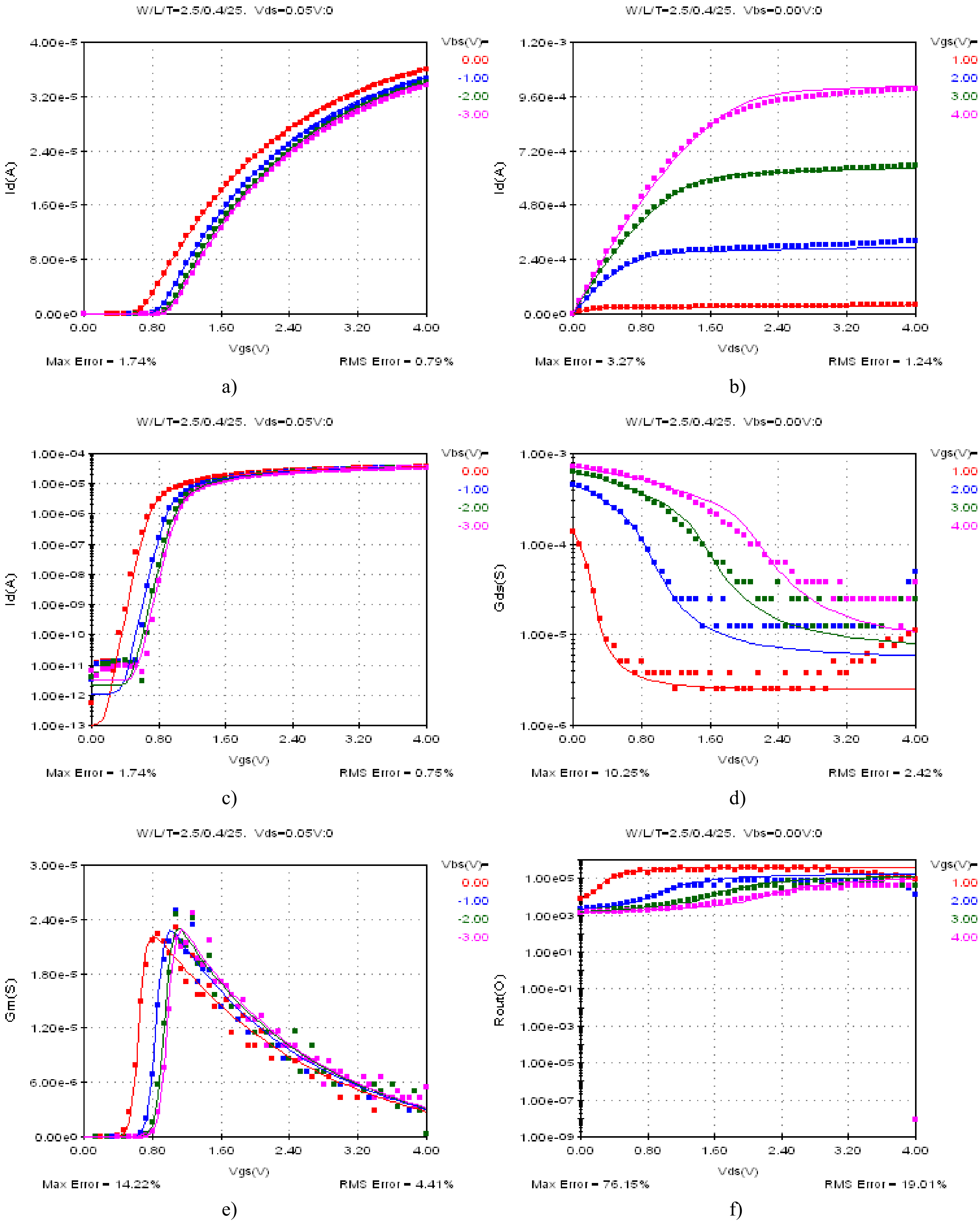


Fig 25 -. L=0.4um W=2.5um NMOS

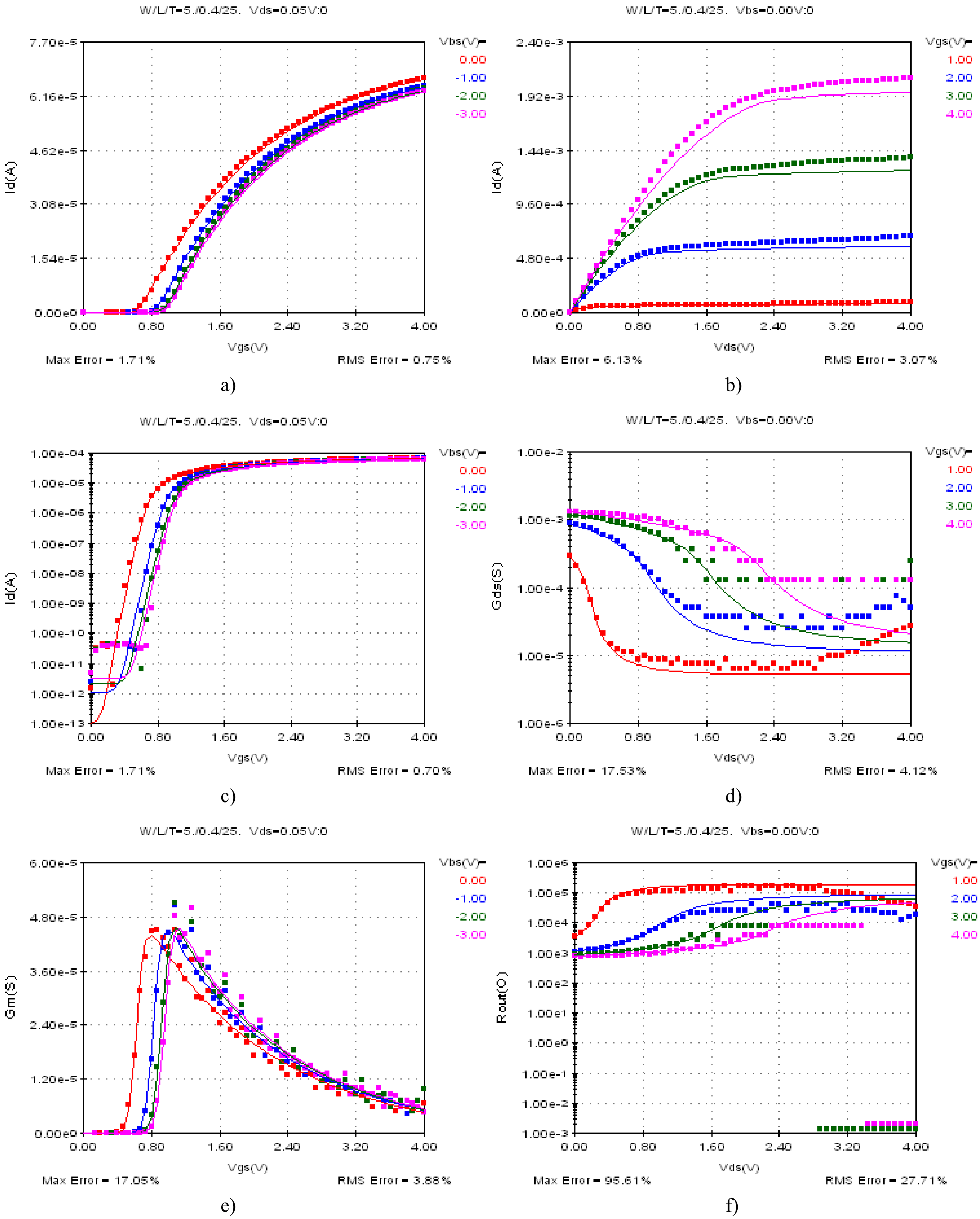


Fig 26 - L=0.4um W=5um NMOS

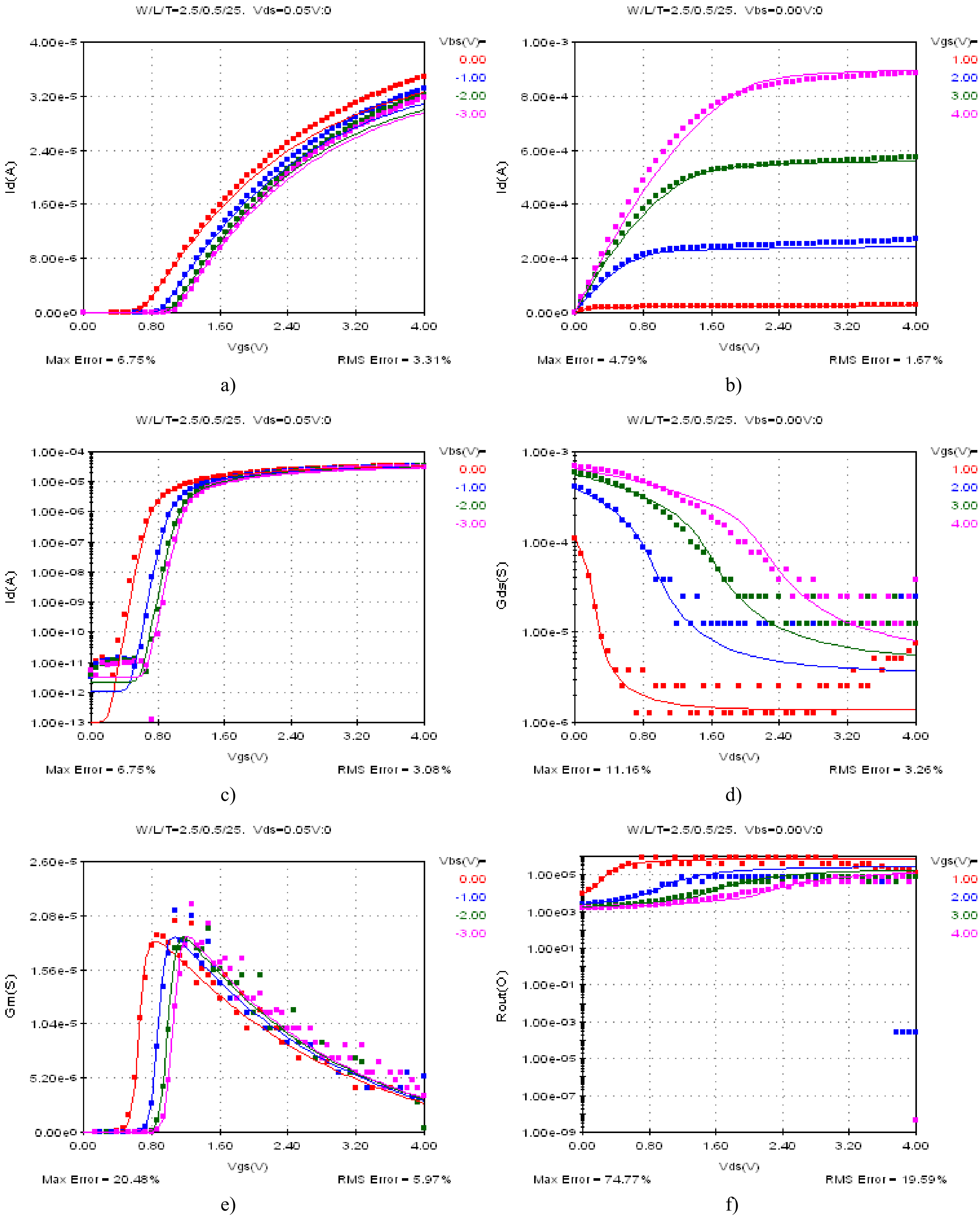


Fig 27 - L=0.5um W=2.5um NMOS

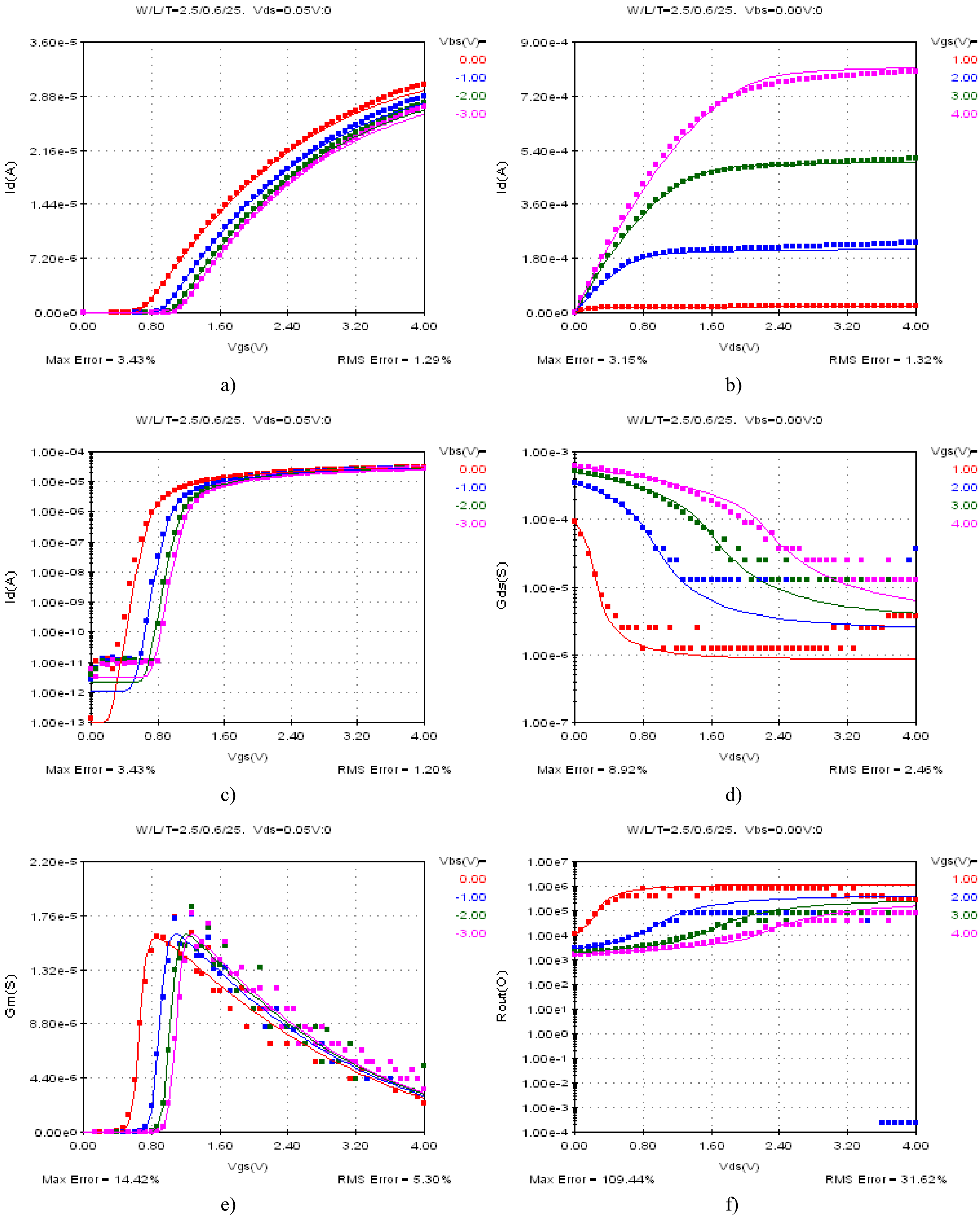


Fig 28 - L=0.6um W=2.5um NMOS

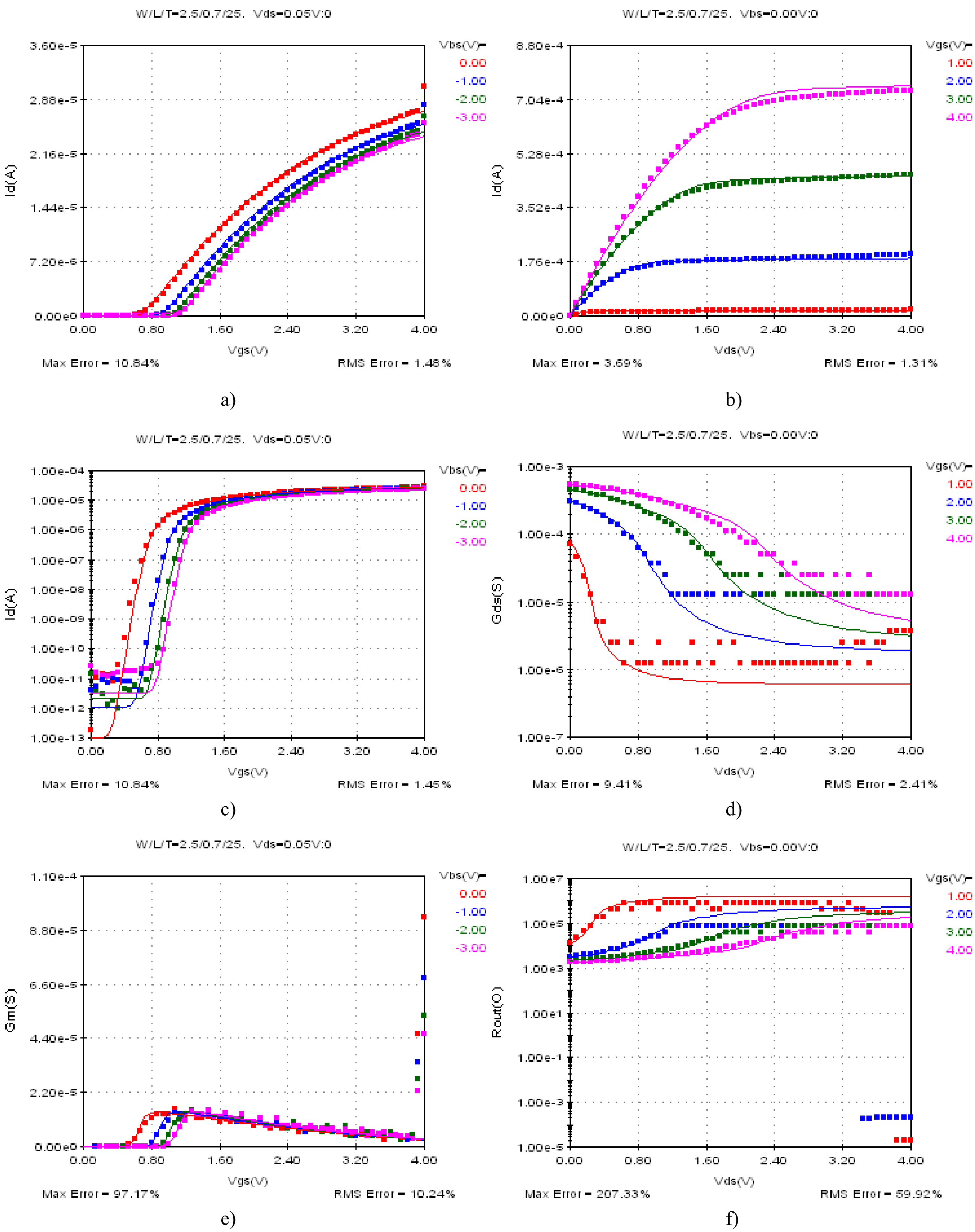


Fig 29 - L=0.7um W=2.5um NMOS

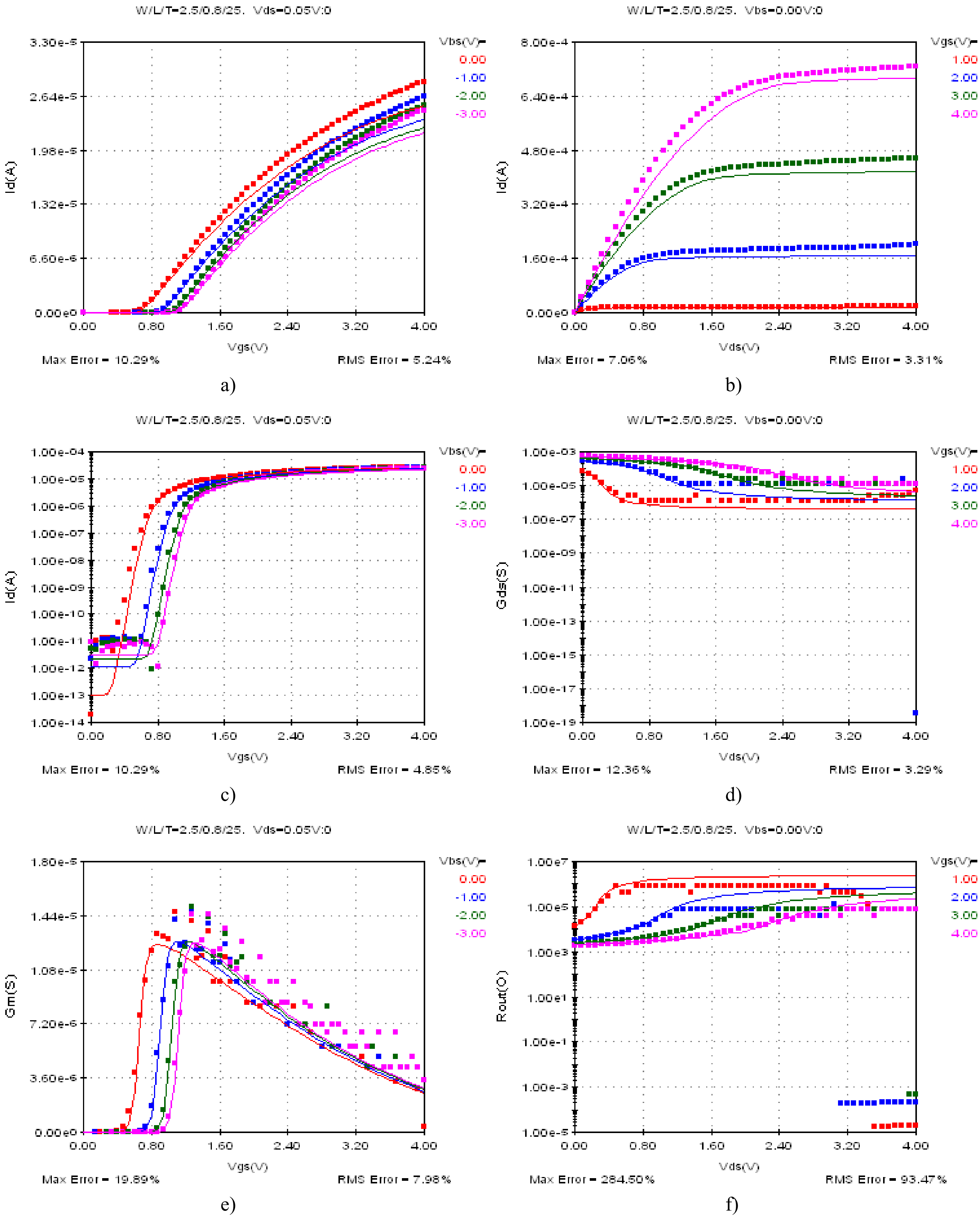


Fig 30 - L=0.8um W=2.5um NMOS

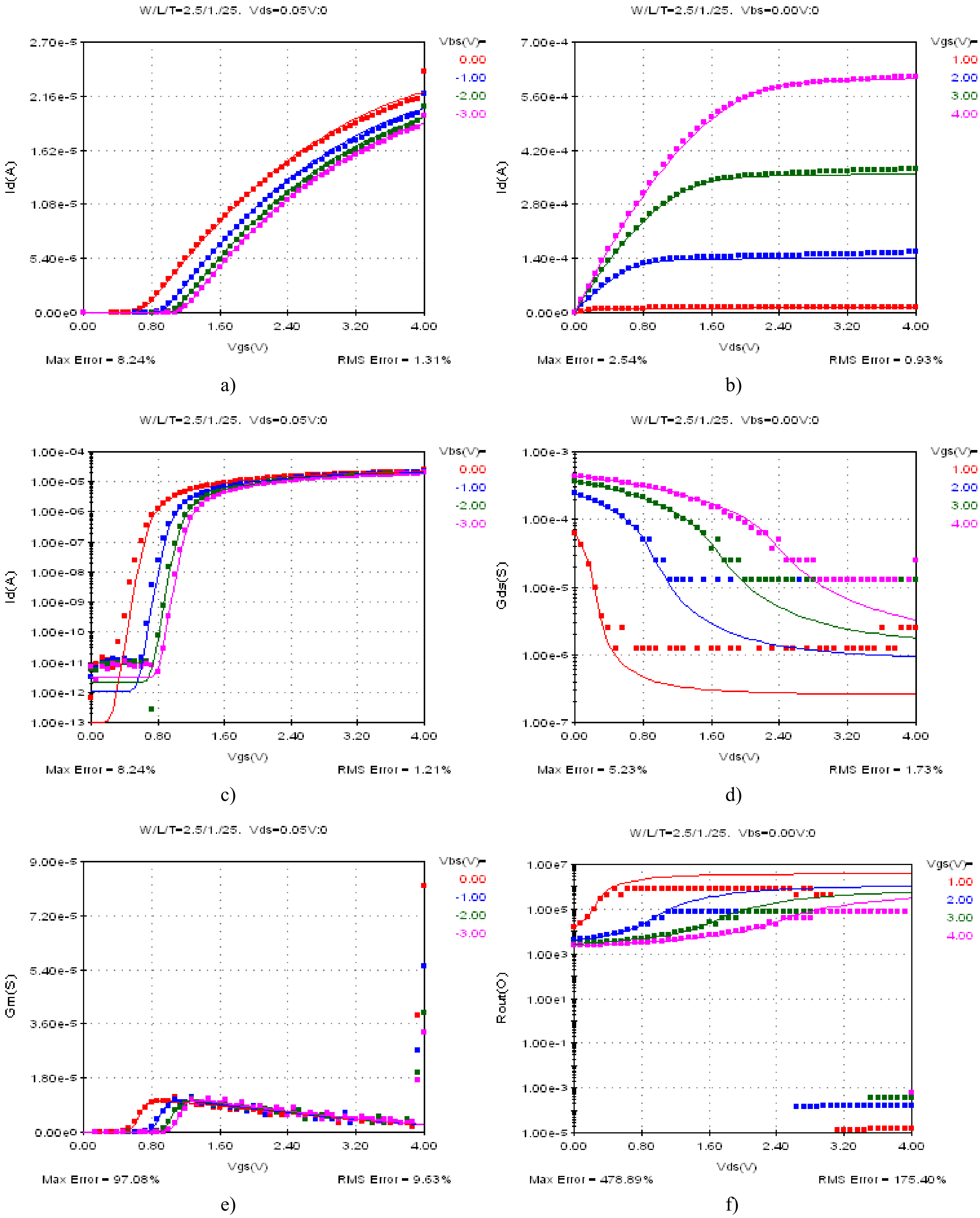


Fig 31 - L=1um W=2.5um NMOS

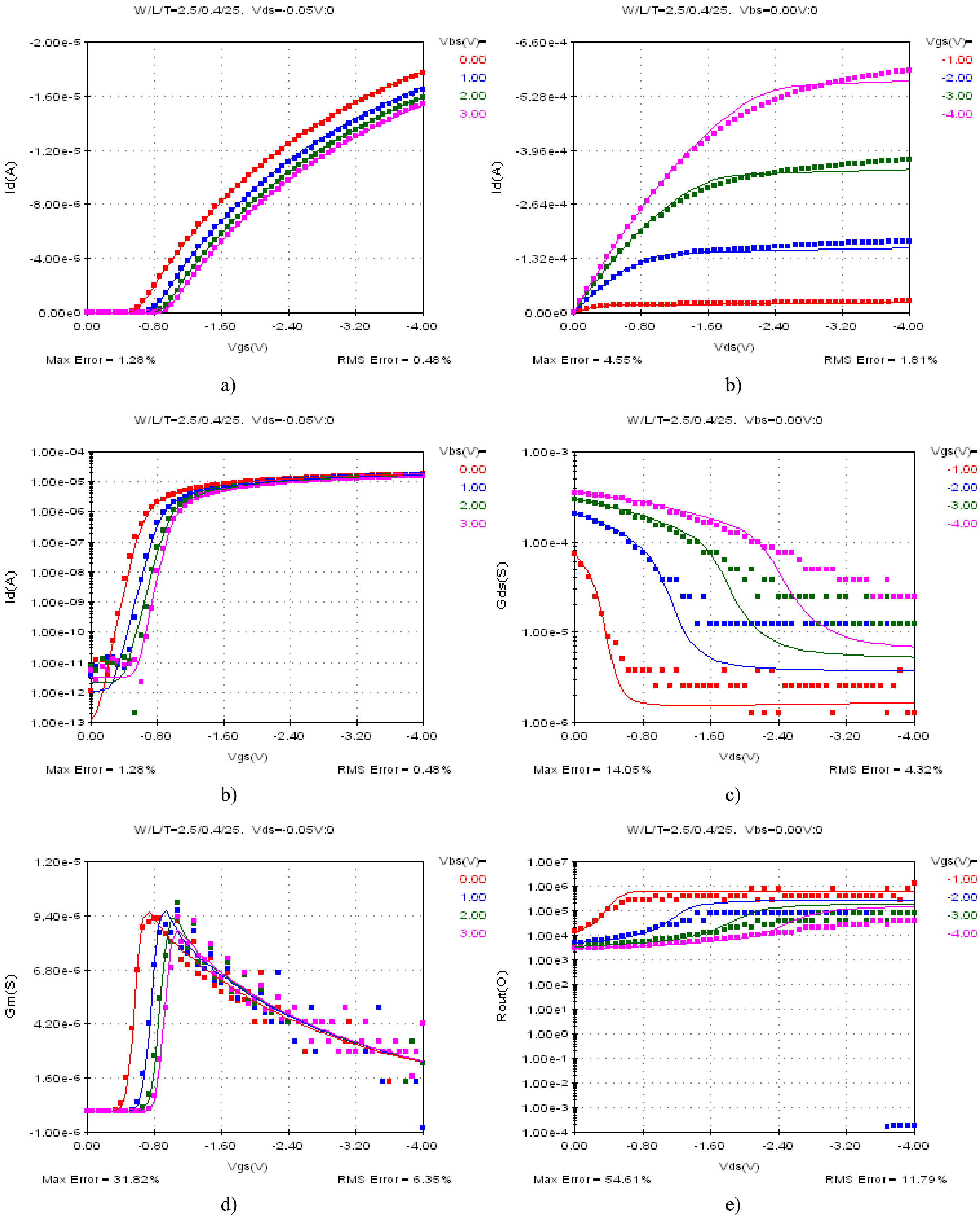


Fig 32 - L=0.4um W=2.5um PMOS

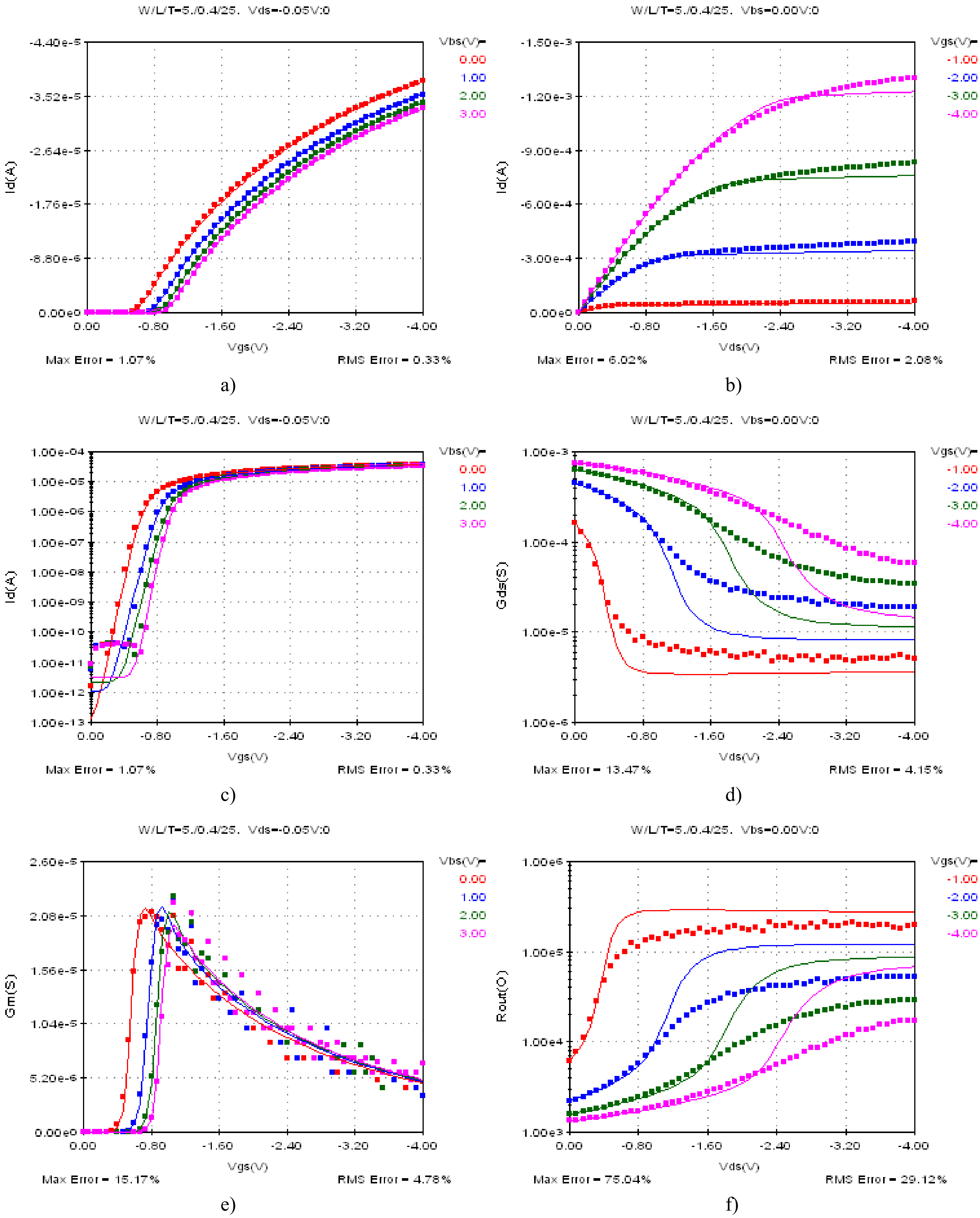
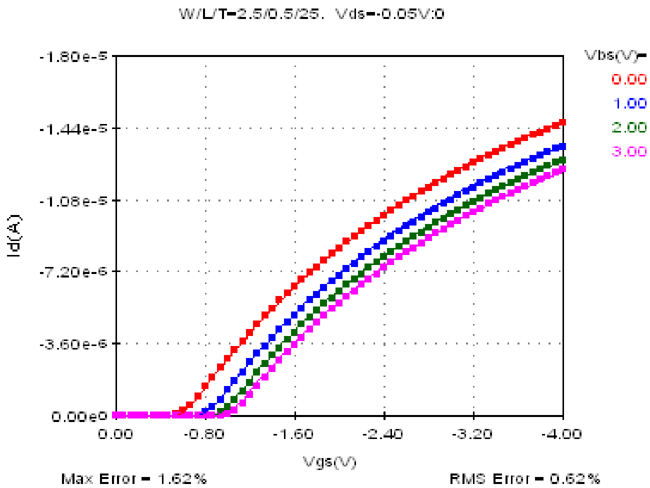
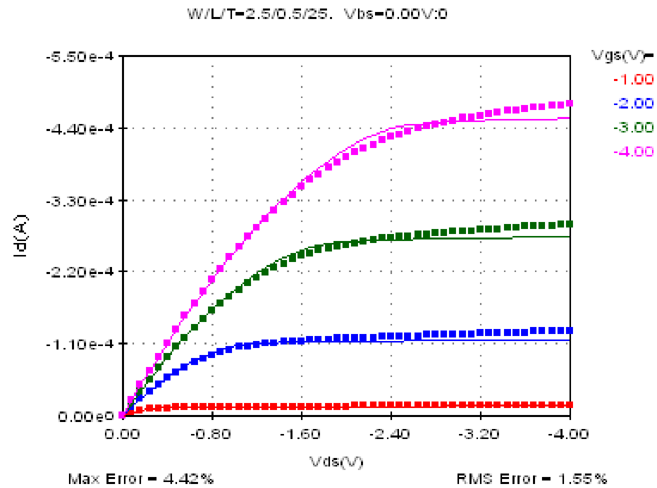


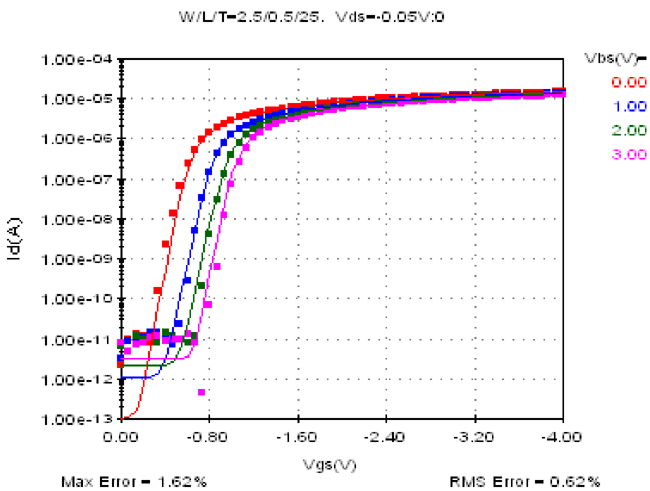
Fig 33 - L=0.4um W=5um PMOS



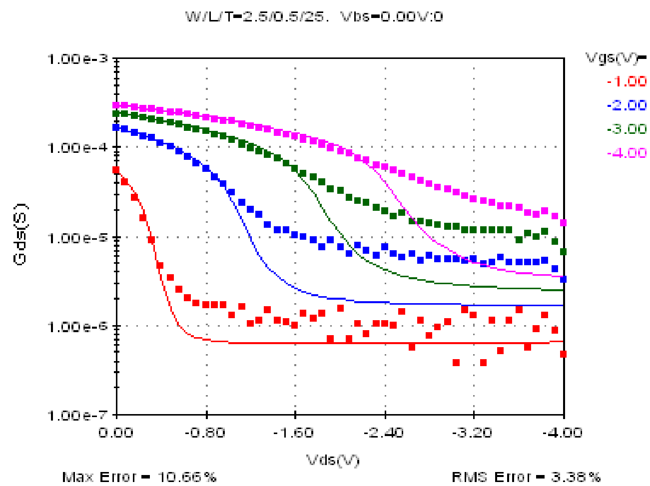
a)



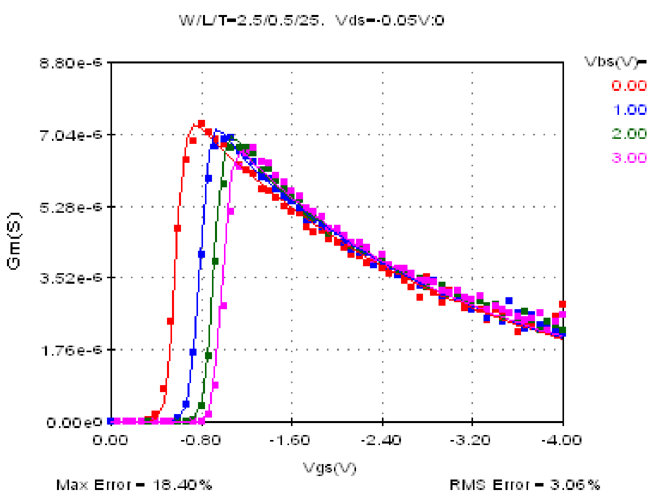
b)



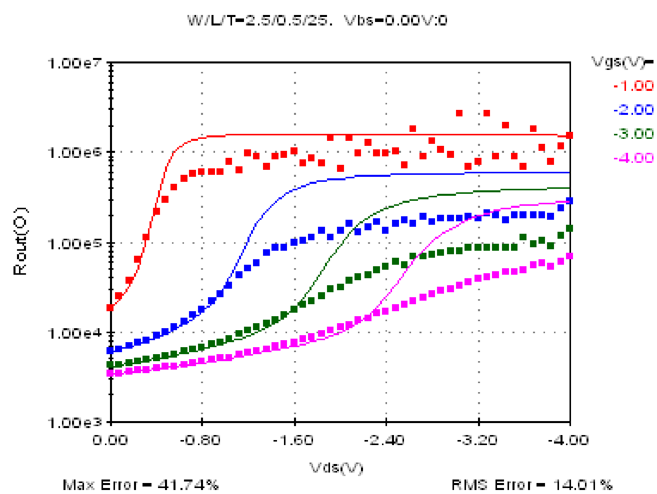
c)



d)



e)



f)

Fig 34 - L=0.5um W=2.5um PMOS

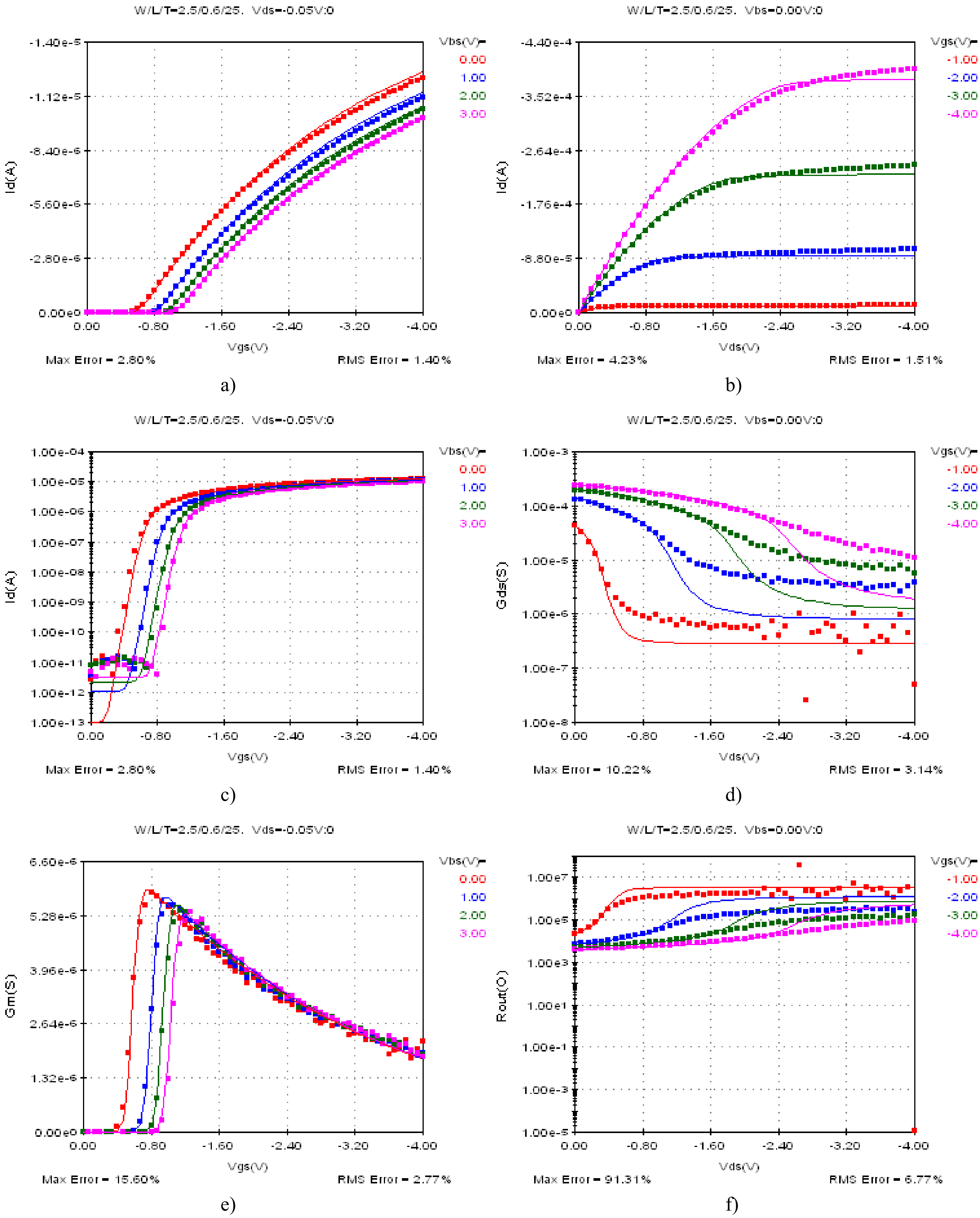
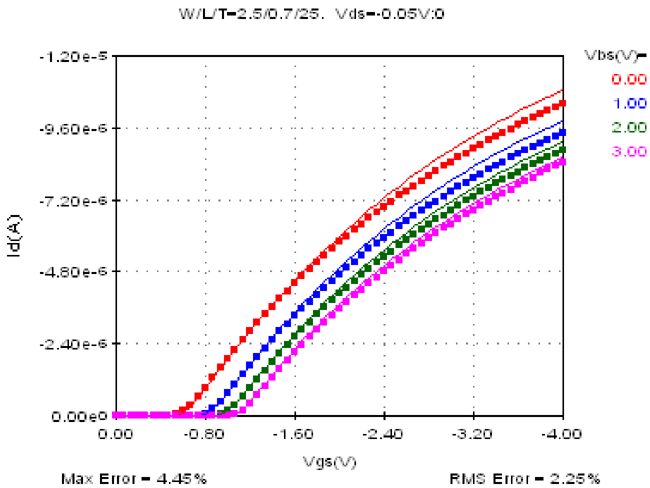
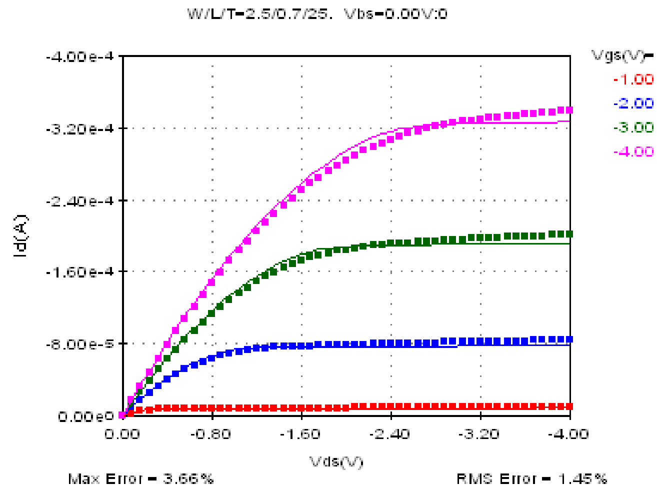


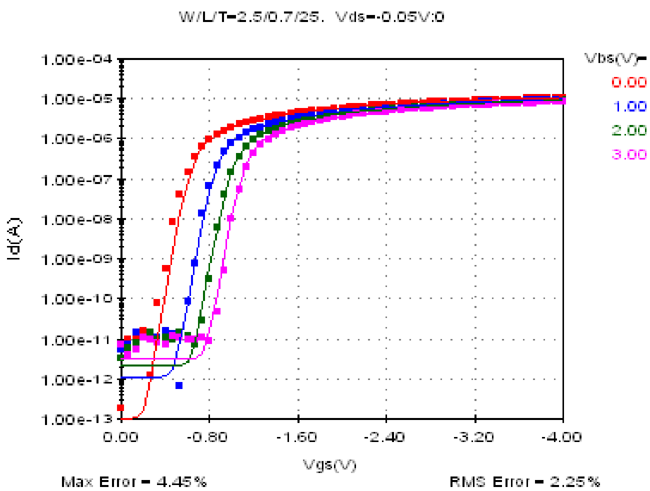
Fig 35 - L=0.6um W=2.5um PMOS



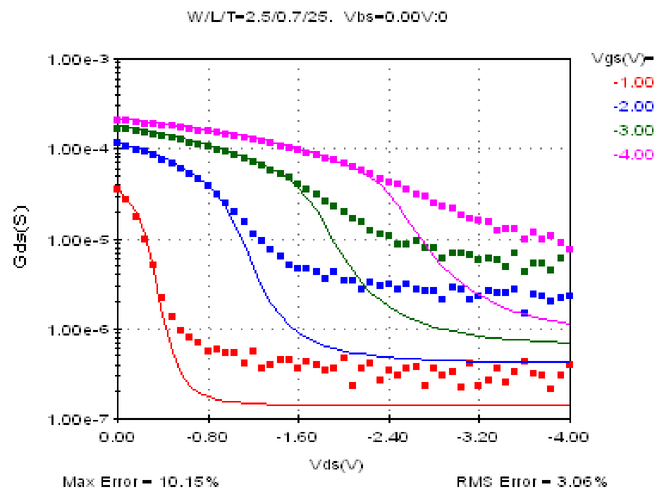
a)



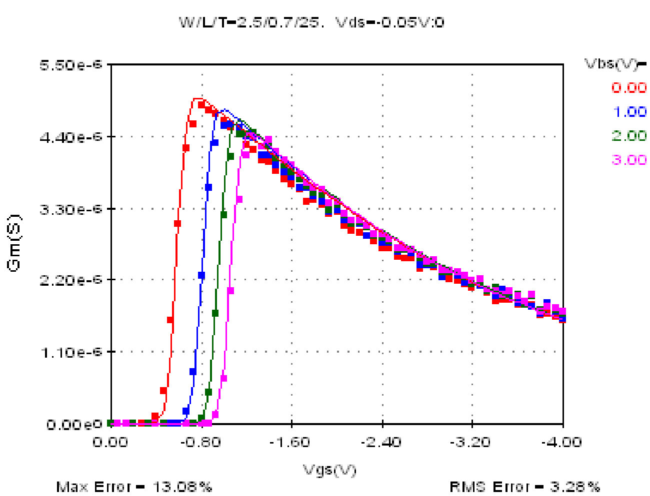
b)



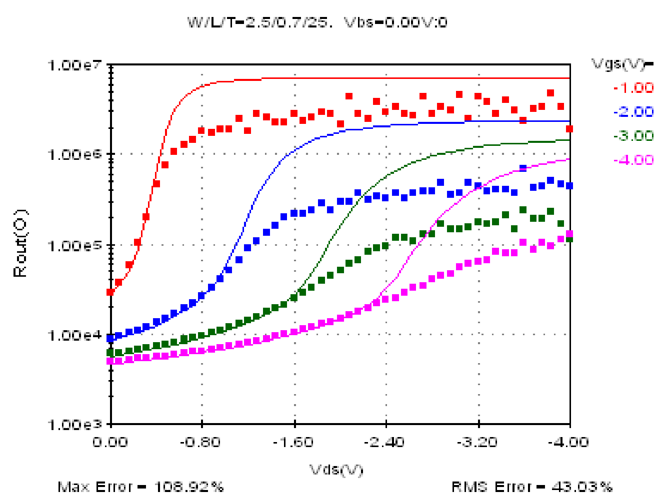
c)



d)

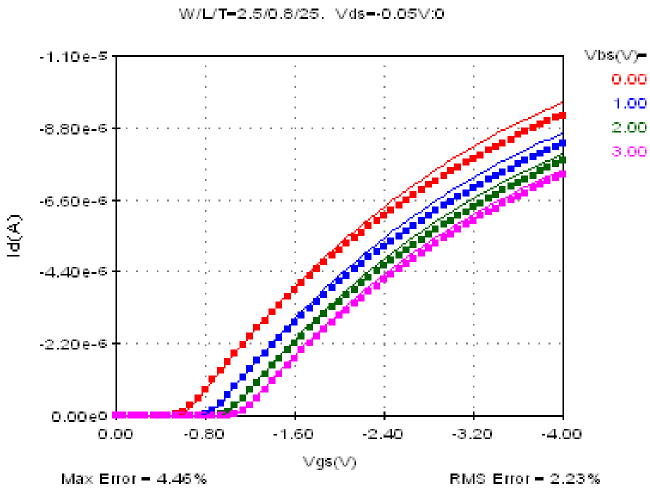


e)

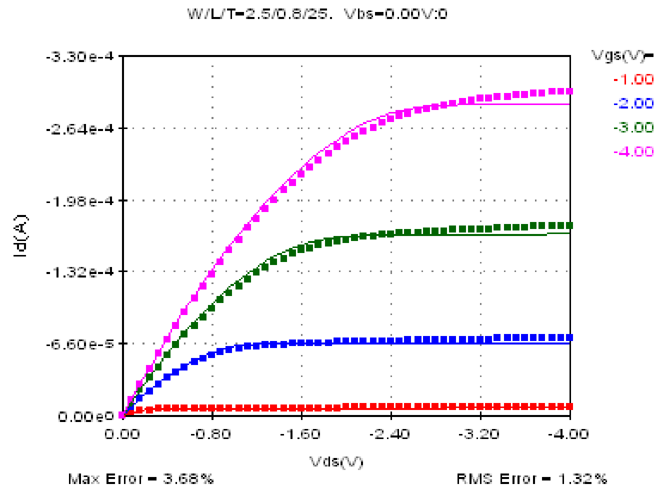


f)

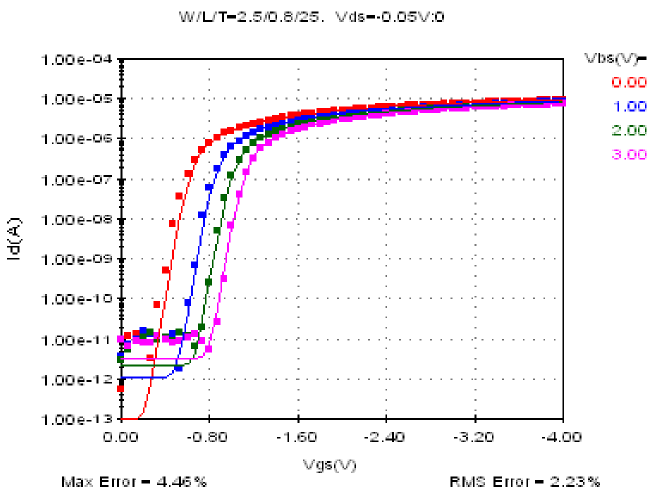
Fig 36 - L=0.7um W=2.5um PMOS



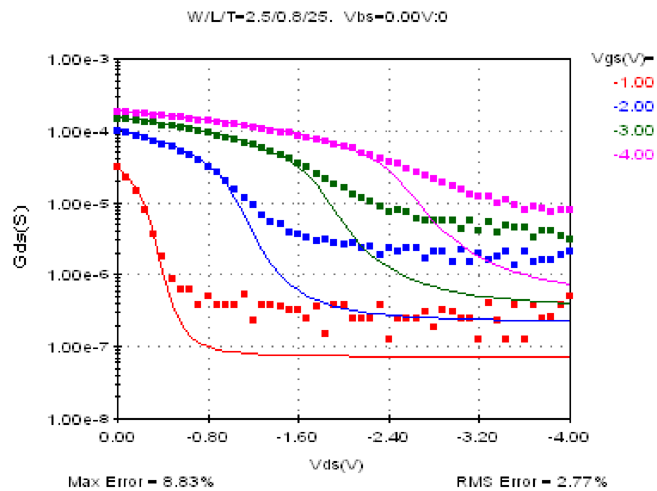
a)



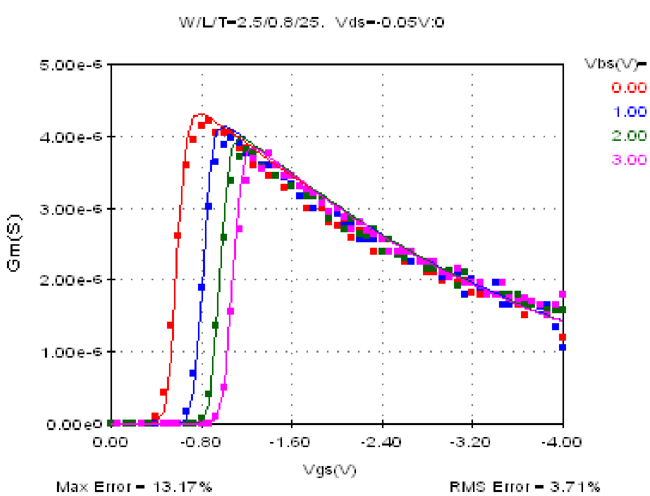
b)



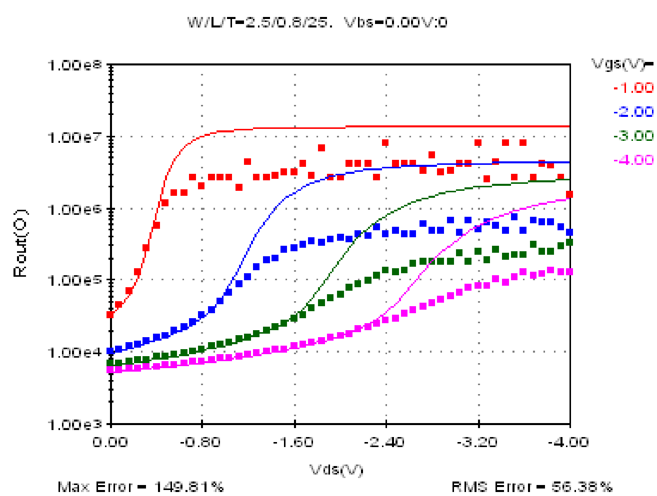
c)



d)



e)



f)

Fig 37 - L=0.8um W=2.5um PMOS

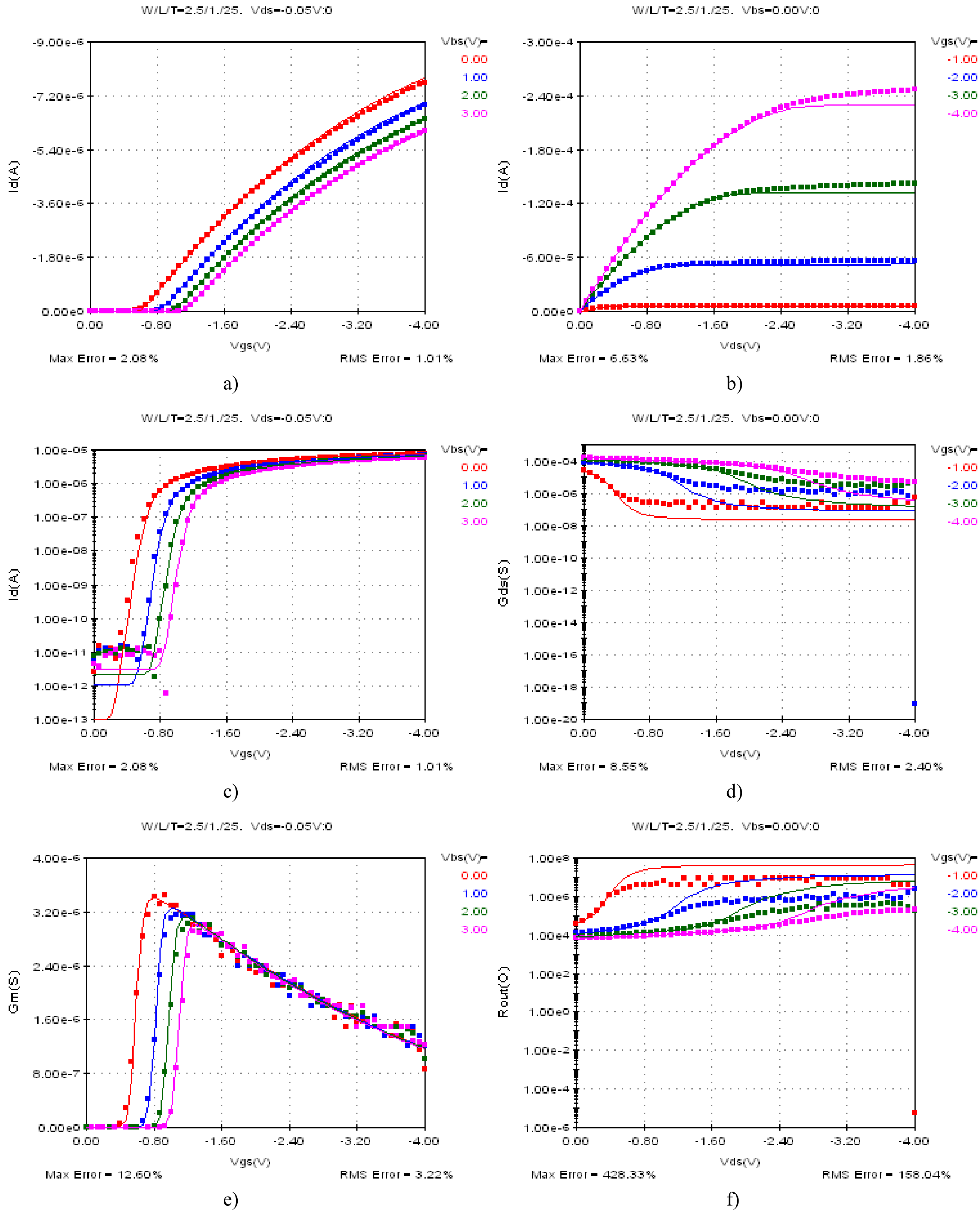


Fig 38 - L=1um W=2.5um PMOS

Appendix F

BSIMPro+ output: Model cards

NMOS Model card

```
*Copyright (C) 1993-2003 Cadence Design Systems, Inc.
* All rights reserved.
simulator lang = spice
simulator lang = spice
.model  default  bsim3v3 type = n
***************************************************************
*                MODEL FLAG PARAMETERS
***************************************************************
+lmin    = 4e-007         lmax    = 1e-006
wmin    = 2.5e-006        wmax    = 5e-006
+version = 3.2            mobmod  = 1
capmod  = 3               nqsmod  = 0
+binunit = 2              stimod  = 0
***************************************************************
*                GENERAL MODEL PARAMETERS
***************************************************************
+tnom    = 25             xl      = 0
xw      = 0               llc     = 0
+lwc     = 0              lwlc    = 0
wlc     = 0               wwc     = 0
+wwlc    = 0              tox     = 8e-009
toxm    = 8e-009          wint    = 5.809148e-008
+lint    = -4.898965e-008 dlc     = 0
dwc     = 0               hdif    = 0
+ldif    = 0              ll      = 2.1097518e-021
wl      = 0               lln     = 1.993408
+wln     = 1              lw      = 0
ww      = -3.454485e-009  lwn     = 1
+wwn     = 0.1            lwl     = 0
wwl     = 0               cgbo    = 0
+cgso    = 0              cgdo    = 0
xpart   = 1
***************************************************************
*                EXPERT PARAMETERS
***************************************************************
+vth0    = 0.6092921       k1      = 1.0400929
k2      = -0.2000714       k3      = 9.784801
+k3b     = -0.8597723      nlx     = 3.714494e-008
dvt0    = 15.932365        dvt1    = 0.5569477
+dvt2    = -0.031210491    dvt0w   = 0
dvt1w   = 0                dvt2w   = 0
+nch     = 6.071564e+017   voff    = -0.06604866
nfactor = 0                cdsc    = 0.0453007
+cdscb   = 0.008908377     cdscd   = 0
cit     = -5.389413e-005   u0      = 0.020214407
+ua      = -1.1641037e-009 ub      = 1.9708006e-018
uc      = -4.537934e-012   ngate   = 1e+030
+xj      = 1.5000001e-007  w0      = 0
prwg    = -0.00018943752   prwb    = -0.030999918
+wr      = 0.7141743       rdsw    = 1309.8905
a0      = 0.7253106        ags     = 0.10746
+a1      = 0               a2      = 0.99
b0      = 1.2044569e-007   b1      = 0
+vsat    = 114124.81       keta    = 0.05579427
dwg     = 0                dwb     = -5.124188e-009
+alpha0  = 0               beta0   = 30
pclm    = 1.003751         pdiblc1 = 0.3274601
+pdiblc2 = 0.0016354327    pdiblcb = -0.1665039
```

```
drout   = 0.56             pvag    = 1
+pscbe1  = 5e+008          pscbe2  = 1e-020
delta   = 0.01             eta0    = 0.012220275
+etab    = -0.009654666    dsub    = 0.1068308
elm     = 5                alpha1  = 0
+vfb     = -0.6320158
**************************************************************
*               CAPACITANCE PARAMETERS
**************************************************************
+clc     = 1e-007         cle     = 0.6
cf      = 0               ckappa  = 0.6
+cgdl    = 0              cgsl    = 0
vfbcv   = -1.247025       acde    = 1
+moin    = 15             noff    = 1
voffcv  = 0
**************************************************************
*               TEMPERATURE PARAMETERS
**************************************************************
+kt1     = -0.11          kt1l    = 0
kt2     = 0.022           ute     = -1.5
+ua1     = 4.31e-009      ub1     = -7.61e-018
uc1     = -5.6e-011       prt     = 0
+at      = 33000
**************************************************************
*               NOISE PARAMETERS
**************************************************************
+noimod  = 1              noia    = 1e+020
noib    = 50000           noic    = -1.4e-012
+em      = 41000000       af      = 1
ef      = 1               kf      = 0
+gdsnoi  = 1
**************************************************************
*               DIODE PARAMETERS
**************************************************************
+rsh     = 0              js      = 0.0001
jsw     = 0               cj      = 0.0005
+mj      = 0.5            cjsw    = 5e-010
mjsw    = 0.33            pb      = 1
+rd      = 0              rdc     = 0
rs      = 0               rsc     = 0
+xti     = 0              n       = 1
pbsw    = 1
**************************************************************
*               STRESS PARAMETERS
**************************************************************
+sa0     = 1e-006         sb0     = 1e-006
wlod    = 0               kvth0   = 0
+lkvth0  = 0              wkvth0  = 0
pkvth0  = 0               llodvth = 0
+wlodvth = 0              stk2    = 0
lodk2   = 1               lodeta0 = 1
+ku0     = 0              lku0    = 0
wku0    = 0               pku0    = 0
+llodku0 = 0              wlodku0 = 0
kvsat   = 0               steta0  = 0
+tku0    = 0
```

PMOS Model card

```
*Copyright (C) 1993-2003 Cadence Design Systems, Inc.
* All rights reserved.
simulator lang = spice
simulator lang = spice
.model  default  bsim3v3 type = p
**************************************************************
*               MODEL FLAG PARAMETERS
**************************************************************
+lmin    = 4e-007         lmax    = 1e-006
wmin    = 2.5e-006       wmax    = 5e-006
+version = 3.2            mobmod  = 1
capmod  = 3              nqsmod  = 0
+binunit = 2              stimod  = 0
**************************************************************
*               GENERAL MODEL PARAMETERS
**************************************************************
+tnom    = 25              xl      = 0
xw      = 0               llc     = 0
+lwc     = 0               lwlc    = 0
wlc     = 0               wwc     = 0
+wwlc    = 0               tox     = 1.5e-008
toxm    = 1.5e-008        wint    = 2.9566223e-007
+lint    = 4.09254e-008    dlc     = 0
dwc     = 0               hdif    = 0
+ldif    = 0               ll      = -2.4660658e-019
wl      = 0               lln     = 1.609413
+wln     = 1               lw      = 0
ww      = -2.7897404e-009  lwn     = 1
+wwn     = 0.1             lwl     = 0
wwl     = 0               cgbo    = 0
+cgso    = 0               cgdo    = 0
xpart   = 1
**************************************************************
*               EXPERT PARAMETERS
**************************************************************
+vth0    = -0.5959         k1      = 0.6308
k2      = -0.04962        k3      = -0.6375571
+k3b     = -0.5528861      nlx     = 0
dvt0    = 2.0494986       dvt1    = 1.1332887
+dvt2    = -0.1532007      dvt0w   = 0
dvt1w   = 0               dvt2w   = 0
+nch     = 6.352297e+016   voff    = -0.06490159
nfactor = 0               cdsc    = 0.00744999
+cdscb   = 0.0020732279    cdscd   = 0
cit     = -5.340484e-005  u0      = 0.01568
+ua      = -4.344e-011     ub      = 4.579e-018
uc      = -8.664e-011     ngate   = 1e+030
+xj      = 2.5e-007        w0      = 0
prwg    = -0.05097421     prwb    = -0.0677802
+wr      = 0.6962816       rdsw    = 1633
a0      = 1.0465789       ags     = 0.09381024
+a1      = 0               a2      = 0.4
b0      = -9.644715e-008  b1      = 0
+vsat    = 380000          keta    = -0.029033011
dwg     = 0               dwb     = 1.7150555e-008
+alpha0  = 0               beta0   = 30
pclm    = 0.009999997     pdiblc1 = 0.009247256
+pdiblc2 = 0.00012325234   pdiblcb = -0.1665039
drout   = 0.56            pvag    = 0
+pscbe1  = 2.8284272e+008  pscbe2  = 1e-020
delta   = 0.01            eta0    = 0.06106803
+etab    = -0.03422515     dsub    = 0.7869266
elm     = 5              alpha1  = 0
+vfb     = -0.6320158
```

```
***************************************************************
*               CAPACITANCE PARAMETERS
***************************************************************
+clc     = 1e-007          cle     = 0.6
cf      = 0                ckappa  = 0.6
+cgdl    = 0               cgsl    = 0
vfbcv   = -0.764456        acde    = 1
+moin    = 15              noff    = 1
voffcv  = 0
***************************************************************
*               TEMPERATURE PARAMETERS
***************************************************************
+kt1     = -0.11           kt1l    = 0
kt2     = 0.022            ute     = -1.5
+ua1     = 4.31e-009       ub1     = -7.61e-018
uc1     = -5.6e-011        prt     = 0
+at      = 33000
***************************************************************
*               NOISE PARAMETERS
***************************************************************
+noimod  = 1               noia    = 1e+020
noib    = 50000            noic    = -1.4e-012
+em      = 41000000        af      = 1
ef      = 1                kf      = 0
+gdsnoi  = 1
***************************************************************
*               DIODE PARAMETERS
***************************************************************
+rsh     = 0               js      = 0.0001
jsw     = 0                cj      = 0.0005
+mj      = 0.5             cjsw    = 5e-010
mjsw    = 0.33             pb      = 1
+rd      = 0               rdc     = 0
rs      = 0                rsc     = 0
+xti     = 0               n       = 1
pbsw    = 1
***************************************************************
*               STRESS PARAMETERS
***************************************************************
+sa0     = 1e-006          sb0     = 1e-006
wlod    = 0                kvth0   = 0
+lkvth0  = 0               wkvth0  = 0
pkvth0  = 0                llodvth = 0
+wlodvth = 0               stk2    = 0
lodk2   = 1                lodeta0 = 1
+ku0     = 0               lku0    = 0
wku0    = 0                pku0    = 0
+llodku0 = 0               wlodku0 = 0
kvsat   = 0                steta0  = 0
+tku0    = 0
```