The first ever university Microlab was built at UCB in 1962.
Please prepare cost estimate for proposed lab for integrated circuits as tentatively shown on the accompanying drawing. Work to be done in Room 432 Cory. Specifications also attached.

Would appreciate discussion prior to submission of cost estimate.

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G & B Routing

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Date: 5 March 62

Deliver to: R. Talcott, 471 Cory Hall
Send order copy to: D. Rudolph, 179 Cory

Date wanted: 23 March 1962
First Surface Acoustic Wave Device (SAW)
F.W. Vollmer, Prof. White 1965

Ultrasonic Flexural Plate-Wave Oscillator Sensor
S.W. Wenzel, Prof. White 1988

Surface acoustic wave delay line for operation at 9 MHz.

Substrate: lead zirconate-titanate ferroelectric ceramic (PZT-5H).

Transducing electrodes: Aluminum.

Electromechanical coupling factor: \( K^2 = 0.043 \) (strongly piezoelectric-polled normal to propagation surface).

Rayleigh surface wave velocity: Approximately \( 2 \times 10^3 \) m/s.

For chemical vapor sensing experiments, we use a teflon cap (white piece on top) to create a small sealed cavity, through which we flow gases via nozzles in the base. Electrical cables connect the device to an external feedback amplifier, to make an ultrasonic oscillator operating at a few MHz, and monitoring equipment.
Piezoelectric Field-Effect Transistor Strain Transducers
J. Conrigan, Prof. Muller 1969

Completed Set of Three CdS TFTs on a 1 X 3 inch slide

A Te PZT-5A Device in Strain Apparatus

Silicon-wafer layout of PI-DMOS Transducers and IDT Pairs.

Piezoelectric Diffused MOS Strain Transducer
K.W. Yeh, Prof. Muller 1976

The top view of a PI-DMOS Transducer

IC-Compatible Piezoelectric Accelerometer
G.L. Halac, Prof. Muller 1982
High Speed Change Redistribution MOS A/D Converter

J. McCreary, Prof. Gray - 1974
N-Channel MOS Operational Amplifier

High Gain Low Offset – K. Burns, J. P. Tsividis, Prof. Gray, 1976
NMOS 5th Order Switched Capacitor Ladder Filter

D. J. Alstott, Prof. Gray - 1977
NMOS 3rd Order Programmable Switch-Capacitor Filter

D. J. Alstott, Prof. Gray - 1978
NMOS 12-Bit Inherently Monotonic A/D Converter

B. Fotouhi, Prof. Hodges - 1978
First Echo Canceller for Integrated Services Digital Network

O. Agazzi, Prof. Hodges - 1981
Self-Calibrating 15-Bit A/D Converter
H. S. Lee, Prof. Hodges - 1982
New Microlab built in 1982

Ready for students - 1983
NMOS Segmented Video D/A Converter

Vivian Shen, Prof. Hodges - 1983
256 KHz Bandpass Switched Capacitor Filter

CMOS 12-Bit A/D Algorithmic Converter

P.W. Li, Prof. Gray - 1983
First CMOS Test Chip Fabricated in the New Microlab by Students of the EE 290 Class
Profs. Neureuther & Oldham, 1983-84
First NMOS Test Chip, Including a 512x8 Bit RAM, Made in the New Microlab

P. W. Li, P. Ruetz, Profs. Brodersen & Gray - 1984
Superconducting Two-Bit Gray-Code to Natural Binary Decoder, Lead-Alloy Process
J. Spargo, Prof. Van Duzer - 1984
Superconducting Four-Bit A/D Converter Using Lead-Alloy Process
H. Ko, V. Nandakumar, D. Petersen, Prof. Van Duzer - 1984
Symbolic Processing Using Riscs:

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- Pipelined Processor Architecture
- On-Chip Instruction & Data Cache
- Multiprocessor Support
- 1.2-2.0 μm CMOS Technology

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FALL 1984
EECS 241
CS 250

SPRING 1985
CS 254

FOR MORE INFORMATION, CONTACT:
Prof. David Hodges
401-A Cory
2-3948

Prof. Randy Katz
523 Evans
2-8778

Prof. David Patterson
527 Evans
2-6587
Pipeline 9-Bit CMOS A/D Converter

S. H. Lewis, Prof. Gray - 1986
Wide Band, Low Noise, Matched Impedance Amplifier in Submicron NMOS Technology

K.Y. Toh,
Prof. Meyer - 1986
CMOS
250 Mb/s
Crosspoint Switch

H. J. Shin,
Prof. Hodges
1987
Superconductive Picosecond Pulse Sampler, Lead-Alloy Process

D. Peterson, Prof. Van Duzer - 1988
Superconducting Three-Bit A/D Converter Using Lead-Alloy Process

D. Petersen, Prof. Van Duzer - 1988
Siemens Star (Experimental Results)

- 0.4 & 0.5 μm Siemens Stars (upper left corner of die).
- 0.3 μm MicroPosit 2400 resist on bare silicon, exposed 11/22/88.
- $\lambda = 0.25 \, \mu m$, $NA = 0.35$, $\sigma = 0.5$, Focus Step = 0.5 μm.

“BEST” EXPOSURE

Optical Lithography Simulation & Its Application to Stepper Characterization

Exposure Target Experiment

K.H. Toh, Prof. Neureuther - 1988
Focus Targets (Experimental Results)

Optical Lithography Simulation & Its Application to Stepper Characterization

Focus Target Experiment

K.H. Toh, Prof. Neureuther - 1988
SIMPL – DIX Layout & Cross-Section of a CMOS DRAM Structure

A.S. Wong, Prof. Neureuther - 1988
CMOS Test Chip for Automatic Data Extraction for Process Modeling

P.M. Kruger, Prof. Hodges - 1988
High-Energy Radiation Detector with Charge-Sensitive Preamplifier Implemented on the Same Substrate

Steve Holland (LBL) - 1989
Thermal Absolute Pressure Gauge with On-Chip Signal Processor

C. Mastrangelo, Prof. Muller - 1990
Surface Micromachined, Force-balance Accelerometer
With On-chip $\Sigma - \Delta$ Modulator Using MICS Process

Weijie Yun, Profs. Howe & Gray - 1991
SQUID Magnetometer
Fabricated from the High $T_c$ Superconductor $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ by Laser Deposition

Integrated CMOS Micromechanical Resonator Oscillator

Clarke Nguyen, Prof. Roger Howe - 1993
Chip Layout of a New Set of Electrical Test Structures Designed for Autoprobe Measurement

David Rodriguez - 1994
MOLDED POLYSILICON THERMALLY ACTUATED TWEEZERS WITH INTEGRATED CONDUCTING, SEMICONDUCTING, AND NON-CONDUCTING BEAMS

80 μm tall beams with electroless nickel, doped polysilicon, or undeoped polysilicon composition

Chris Keller/Roger Howe
Device Structure

Horizontal Double Gate

Vertical Double Gate (FinFET)
TEM Profile of Si-Fins

Planarized gate
Si-Fins
Buried Oxide

a-a’ cross-section

SiN
Fin
BOX

20 nm
**I-V Characteristics** \( (L_G=60\text{nm}, \ W_{fin}=40\text{nm}, \ T_{ox}=2.5\text{nm}) \)

- **NMOS** \( I_{on} = 500\text{uA/um} \) @ \( V_g - V_t = 1\text{V} \) and \( V_d = 1\text{V} \)
- **PMOS** \( I_{on} = -400\text{uA/um} \) @ \( |V_g - V_t| = 1\text{V} \) and \( V_d = -1\text{V} \) or
- **NMOS** \( I_{on} = 1\text{mA/um} \) and **PMOS** \( I_{on} = -0.8\text{mA/um} \) for the definition of double gate channel width.
Drive Current vs. Extension Length

- Smaller gap shows higher drive current.
SEM for $L_g=15\text{nm}$ and $W_{\text{fin}}=10\text{nm}$

- The smallest MOSFET all over the world!
I-V Characteristics ($L_g=15\text{nm}$, $W_{\text{fin}}=10\text{nm}$, $T_{\text{ox}}=2.1\text{nm}$)

**NMOS** $I_{on}$ is 400uA/um @ $V_g-V_t=1\text{V}$ and $V_d=1\text{V}$

**PMOS** $I_{on}$ is -330uA/um @ $|V_g-V_t|=1\text{V}$ and $V_d=-1\text{V}$ or $|V_g-V_t|=1\text{V}$ and $V_d=1\text{V}$

**NMOS** $I_{on}$ is 800uA/um and **PMOS** $I_{on}$ is -660uA/um for the definition of double gate channel width.