INVESTIGATION OF A SPIN-ON DIELECTRIC AS AN INTERLAYER DIELECTRIC FOR THE MARVELL NANOFABRICATION LABORATORY CMOS210 BASELINE PROJECT

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2014 TRANSFER TO EXCELLENCE RESEARCH PROGRAM
• Multilevel metallization schemes consist of multiple levels of metal traces that interconnect one another in selected locations. Areas where they do not connect are isolated by placing an insulating, interlayer dielectric material between them.
• The goal of this project is to investigate IC1-200 and its use as a first level interlayer dielectric (ILD).
HOW IS THIS DONE?

Spin-on Dielectric

Low Temperature Oxide

Chemical Mechanical Polishing

(svgcoat3) – spin coater

(tystar12)-LPCVD furnace

(cmp) – chemical mechanical polisher
HOW DO WE KNOW IT IS SUCCESSFUL?

METROLOGY

(ellips) – Film Thickness

(leo) – Cross-Sectional SEM Profiles

nanoduv – Film Thickness
EXPERIMENTAL PROCESS FLOW

1. Obtain Wafers with Si Topography
2. Deposit First Low Temperature Oxide Film
   3a. Spin Coat Spin-On Dielectric
   3b. Cure Spin-On Dielectric
   4a. Anneal Spin-On Dielectric
   4b. Deposit Second Low Temperature Oxide Film
5. Chemical Mechanical Planarization
EXPERIMENTAL – 1. OBTAIN WAFERS

- Bare Si topo wafers are developed through a photolithography and dry etching process.
EXPERIMENTAL – 2. DEPOSIT FIRST LOW TEMPERATURE OXIDE

1000 Å of low temperature oxide using LPCVD furnace
• 450 °C
• 9.5 minutes
• 107 Å/min

Lower LTO Thickness (nanoduv)

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Center (Å)</th>
<th>Flat (Å)</th>
<th>Top (Å)</th>
<th>Right (Å)</th>
<th>Average (Å)</th>
<th>Uniformity</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>1161</td>
<td>1168</td>
<td>1158</td>
<td>1167</td>
<td>1162</td>
<td>0.008605852</td>
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<tr>
<td>6</td>
<td>1133</td>
<td>1141</td>
<td>1060</td>
<td>1139</td>
<td>1082</td>
<td>0.074861368</td>
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<tr>
<td>9</td>
<td>1117</td>
<td>1133</td>
<td>1098</td>
<td>1140</td>
<td>1114</td>
<td>0.037701975</td>
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<td>12</td>
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<td>1127</td>
<td>1145</td>
<td>1142</td>
<td>1140</td>
<td>0.019298246</td>
</tr>
</tbody>
</table>

Average Thickness (Å) 1125
Average Uniformity 0.03511686

The LTO deposition target = 1000 Å
Average LTO deposition = 1134 Å
Spin coat ~1400 – 4000 Å
Spin-on Dielectric
• 500 RPM for 5 s
• 800 RPM for 40 s
• 100 °C for 60 s
• 200 °C for 60 s
• 400 °C for 30 min
Cross-Sectional Scanning Electron Microscope Image (Low Temperature Oxide and Spin On Dielectric)
EXPERIMENTAL – 4. DEPOSIT SECOND LOW TEMPERATURE OXIDE FILM

In the field region, the spin-on dielectric is ~4,000 Å and the first LTO is ~1,100 Å. Thus, the second layer of LTO is ~20,300 Å.

<table>
<thead>
<tr>
<th>LTO/Spin-on Dielectric/LTO Stack Thickness</th>
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<tbody>
<tr>
<td>Position</td>
</tr>
<tr>
<td>Thickness</td>
</tr>
</tbody>
</table>

20,000 Å LTO deposited
• 450 °C
• 187 min
• 107 Å/min deposition rate
EXPERIMENTAL – DEPOSIT SECOND LOW TEMPERATURE OXIDE FILM

Second Low Temperature Oxide

Spin-on Dielectric

First Low Temperature Oxide

Second Low Temperature Oxide

Spin-on Dielectric

First Low Temperature Oxide
Blisters and cracking occurred as a result of outgassing.

Spin-on Dielectric outgassing occurs when volatile organic materials (CO₂, and water) evolve from the spin-on dielectric.
Optimized Recipe Conditions:
- Ramp Time = 5 min
- Load Temp = 465 °C
- Center Temp = 465 °C
- Source Temp = 465 °C
- Anneal Time = 40 min

The annealing recipe was optimized to spend ~ 1 hour above 450 °C and ramp up/down to/from 465 °C as quickly as possible.
The modification on the vacoven to perform a 450 °C cure and the addition of a 465 °C anneal in tystar12 resulted in LTO films of better quality.

- 30 min, 400 °C, 200 – 400 torr cure in vacoven before LTO deposition (no anneal).
- 60 min, 450 °C, 200 – 400 torr, cure with 5 dehydration loops in vacoven, followed by an anneal at 465 °C for 40 min before LTO dep.
FUTURE WORK: CHEMICAL MECHANICAL PLANARIZATION

First Low Temperature Oxide

Spin-on Dielectric

Second Low Temperature Oxide Polished to ~7000 Å using chemical mechanical polisher

### EXPERIMENTAL – 5. CHEMICAL MECHANICAL PLANARIZATION

<table>
<thead>
<tr>
<th>Time (120 s intervals)</th>
<th>Removal Rate(Å /min)</th>
</tr>
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<tbody>
<tr>
<td>1st</td>
<td>32.13</td>
</tr>
<tr>
<td>2nd</td>
<td>31.82</td>
</tr>
<tr>
<td>3rd</td>
<td>30.4</td>
</tr>
<tr>
<td><strong>Average Removal Rate</strong></td>
<td><strong>31.45</strong></td>
</tr>
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</table>
CONCLUSION

• IC1-200 spin-on dielectric was investigated as a first level interlayer dielectric (ILD).

• A three layer stack, consisting of 1,000 Å low temperature oxide ~1,400 – /4,000 Å spin-on dielectric/20,000 Å low temperature oxide has been developed for the ILD.

• Outgassing of volatile materials caused blistering which was overcome by developing a new anneal recipe for the LPCVD reactor.
I would like to thank TTE program directors Lea, Sharnia and Lili for making sure that me and the rest of my fellow TTE colleagues had a great experience from arrival to departure and for doing all they can to help us get the most out of this incredible experience.

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