Chapter 3.8

CMOS Baseline Test Chip

1.0 Title

CMOS Baseline Test Chip.

2.0 Purpose

This document provides necessary information for the lab members to incorporate their custom design (layout) into our latest CMOS baseline test chip template. Baseline test chips are regularly fabricated and tested in the Microlab for the purpose of monitoring process tools and/or development of new processes on a new installation, currently good at the 0.35 μm technology node.

3.0 Scope

The CMOS baseline template is populated with individual transistors and other structures, in an L-shaped area, at the top and left sides of the chip. The rest of the chip covers an area of 6 mm x 7 mm (wafer level) for members to piggyback their design, based on our current baseline process. At the end of the fabrication process, the individual transistors and circuits (L-shaped area) gets electrically tested to highlight any possible problem in the lab. Once the E-test is completed, members will get their share of the processed wafers for their own specific test/evaluation (open area of the test chip).

4.0 Applicable Documents

Revision History

4.1 Guidelines for 6” mask generation procedure from your layout design can be found at
http://nanolab.berkeley.edu/labmanual/chap3/3.1cad.pdf

4.2 The latest CMOS baseline test chip template can be found on silicon:
/home/mercury4/cad/baseline/
The template is available in a **gds** or **cif** format.
At silicon prompt, type: **cd /home/mercury4/cad/baseline/**
The technology files for Cadence are also available in the same directory (**.tf** and **.drf** files).

4.3 The 10-pin and the 32-pin measurement pad structures can also be found on silicon:
/home/mercury4/cad/baseline/

4.4 Design rules and detailed process information for the latest Microlab process (0.35 μm technology) is included in the Baseline Reports IV and V available at:

http://microlab.berkeley.edu/baseline/reports/baselinerptIV.pdf

http://www.eecs.berkeley.edu/Pubs/TechRpts/2007/EECS-2007-26.pdf

4.5 Earlier revision of baseline test chip designed for 4” process and the related information are also available on silicon: **/home/mercury4/cad/old_baseline/**
Keep in mind that we no longer fabricate the CMOS baseline test chip on 4" substrate.

5.0 Definitions & Process Terminology

5.1 The following table lists the GDSII layers with their universal assigned layer numbers. Please note that more than one lithography step in our current process uses the same mask. For further details, see the Appendix of this chapter.

Layer Number	GDSII Layer Name
46	Poly
43	Active
49	Metal1
51	Metal2
42	NWell
45	NSelect
44	PSelect
52	PWell
47	PField
48	Active Contact
50	Via1
57	Metal3
58	Via2

5.2 The available area in the drop-in field of the chip which can be occupied by your design is approximately 6 mm × 7 mm. The full chip size is 8.5 mm × 8.5 mm.

5.3 If you plan to take advantage of the available measurement routines and probe cards on the automated probe station (Autoprobe) in the later measurement phase, you have to lay out your devices connected to the pre-defined measurement pad structures. For the location of the 10 and 32-pin measurement pad structures please see Section 4.3 of this chapter.

6.0 Safety

N/A

7.0 Statistical Process Data

N/A

8.0 Available Processes & Gases

N/A

9.0 Equipment Operation

N/A

10.0 Troubleshooting Guidelines

N/A

11.0 Figures & Schematics

N/A

12.0 Appendix

List of the Lithography Steps and the
Assigned Masks up to the First Metal Layer

Please note that the same mask is occasionally assigned for different lithography steps.

Step	Mask
Zero layer photo	Zero layer mask - PM marks
N-well photo	NWELL mask (Dark field)
P-well photo	PWELL mask (Clear field)
Active area photo	ACTIVE mask (Clear field)
P-well field imp. photo	PFIELD mask (Clear field)
NMOS Vt adj. implant photo	PWELL mask Clear field)
PMOS Vt adj. implant photo	NWELL mask (Dark field)
Poly gate photo	POLY mask (Clear field)
P-type LDD implant photo	PSELECT mask (Dark filed)
N-type LDD implant photo	NSELECT mask (Dark field)
P+ Gate & S/D photo	PSELECT mask (Dark filed)
N+ Gate & S/D photo	NSELECT mask (Dark field)
Contact photo	CONTACT mask (Dark field)
New PM marks	Zero layer mask - PM marks
Metal1 photo	METAL1 mask (Clear field)
Via1 photo	VIA1 mask (Dark field)
Opening 4 dies for PM marks	Blank mask
Metal2 photo	METAL2 mask (Clear field)
Via2 photo	VIA2 mask (Dark field)
Opening 4 dies for PM marks	Blank mask
Metal3 photo	METAL3 mask (Clear field)

Note: The P-well mask is the inverse of the N-well mask. The PFIELD mask was created by merging the P-well mask with the ACTV mask.