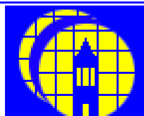
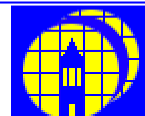


Lab Manual



Chapter 1.6

I - Substrate Specifications

Polished Single-Crystal Silicon, Prime Wafers

(all numbers nominal)

Wafer Specification Table

Diameter	100 mm	4-inch	150 mm	6-inch
Thickness	525 µm	20.5 mils	675 µm	26.3 mils
Primary Flat Length	32.5 mm		57.5 mm	
Secondary Flat Length	18.0 mm		37.5 mm	
Bow, max	40 µm		60 µm	
Wrap, max	40 µm		60 µm	
Total thickness variation (max. Flatness)	10 µm		10 µm	

Table 1- General spec for 4” and 6” substrates

Available silicon wafers at NanoLab stockroom are listed in table2, below.

NanoLab SKU	Size in Inches	Type	Grade	Orientation	Resistivity	Thickness
70255	4”	P	Test	1-0-0	1-50 ohm cm	475-575um
70252	4”	P	Prime	1-0-0	10-30 ohm cm	500-550um
70254	4”	N	Test	1-0-0	0.5-30 ohm cm	475-575um
70251	4”	N	Prime	1-0-0	3-10 ohm cm	500-550um
70259	6”	P	Test	1-0-0	1-50 ohm cm	600-700um or 625-725um
70257	6”	P	Prime	1-0-0	10-30 ohm cm	650-700um
70258	6"	N	Test	1-0-0	0.5-30 ohm cm	600-700um or 625-725um
70256	6"	N	Prime	1-0-0	3-10 ohm cm	650-700um

Table 2 - available wafers in stockroom and their specification

Note: NanoLab offers wafers with one major flat (SEMI standard) due to the fact that the majority of our automated equipment are set up to accept wafers with single flat, only (no minor flat). This includes: AMAT Centura, STS, and lam etchers, as well as ASML, GCAWS2 and GCAWS6 steppers in the lab.

SEMI standard major flat size is defined as:

For 4- inch wafers flat length (mm) = 37.5 (+2.5)

For 6-inch wafers flat length (mm) = 57.5 (+2.5)

II - Processing Notes

1. ***Class Wafers*** **–** A large variety of glasses are available with different metal-oxide contents. Please refer to chapter 1.15 MOD 31 for more detail. NanoLab stocks borofloat and fused silica (known as quartz) wafers. You can obtain other type of glass wafers from vendors. Please keep in mind your wafers will need to have single flat (SEMI standard specification) much like regular silicon substrates (above table), if you are going to use them on any of the automated tools in the lab. Wafer flatness may be an issue, if lithography steps are to be done on ASML stepper. This tool requires less than 70 um height variation across a 6-inch wafer, otherwise wafer handling will be a problem on this particular tool. For more information about glass wafer processing follow our chapter 1.15 link at:
   http://nanolab.berkeley.edu/labmanual/chap1/1.15processmods.pdf

2. ***Scribing wafers***- Members often need to diamond scribe their wafers for identification. Do NOT scribe wafers on their back, if you are going to send them through any of the etchers with electrostatic chucks, as well the ASML stepper. The wafer handler on ASML300 stepper cannot handle wafers with deep scratch marks on their back. Best practice is to lightly scribe the top near the flat on your wafers.

III - Sorting Unlabeled Silicon Wafers

The quality, resistivity type, bulk resistivity, and crystal orientation of unidentified Si wafers can be determined if the wafers are new (unused). The following is a description of the procedures to follow for identifying "unknown" wafers.

1. *Bright Light Inspection*

(1) Inspect all wafers under the bright light in V1 (VLSI area).

(2) Discard any badly scratched or very hazy wafers.

2. *Determining Resistivity Type*

Use MILLER DESIGN FPP-5000 (4ptprb) to measure resistivity type.

(1) Place the wafer, unpolished (dull) side up, over the probe opening.

(2) Depress the button (don't touch the wafer with fingers, tweezers, or vacuum wand while testing).

(3) N or P for dopant type will be displayed.

Consult the manual for VECCO FPP 4-POINT chapter 8.1 for more detailed instruction

3. *Measuring Bulk Resistivity*

Use MILLER DESIGN FPP-5000: Please see the instruction posted in Chapter 8.1 and the SLICE option of the tool with proper wafer thickness to be entered under the PRGM mod. Consult the manual for VECCO FPP 4-POINT chapter 8.1 for more detailed instruction

Determine Crystal Orientation

Using a diamond scribe and tweezers, cleave one wafer from each box. This is a destructive method.

(1) With a diamond scribe, make a small nick in the wafer at the major flat.

(2) Apply pressure to the nicked area with tweezers in order to cleave the wafer.

(3) Make another nick in the cleaved piece and repeat step 2.

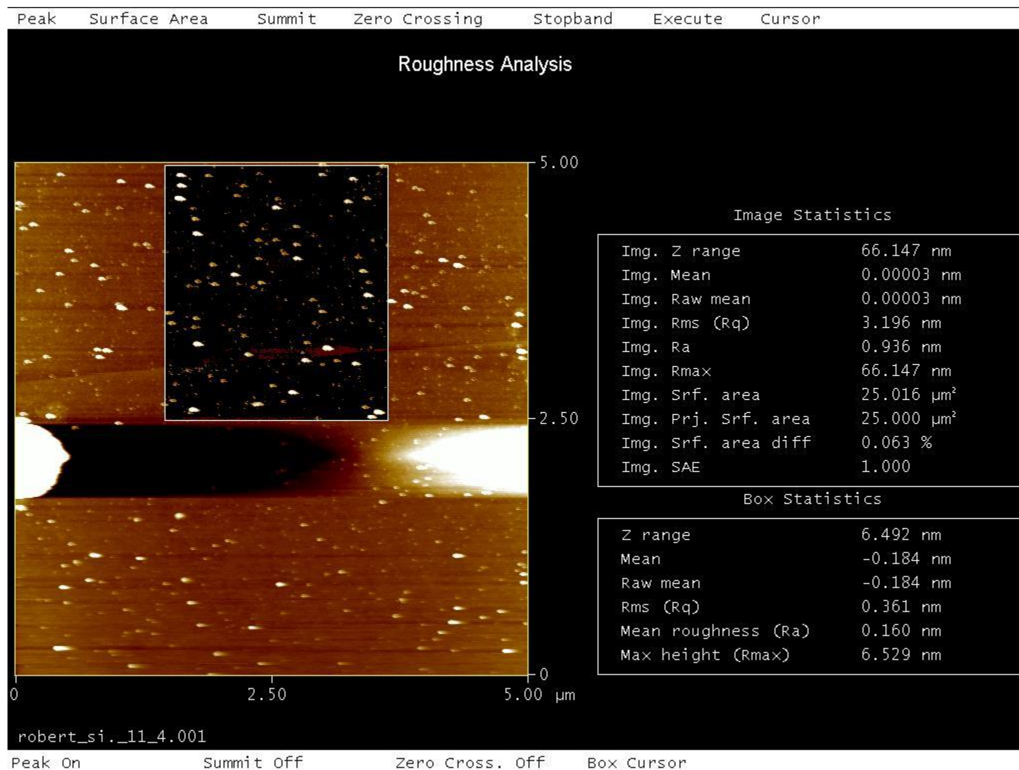
(4) If the cleaved pieces form rectangles (cleave at 90 deg. angles), then the crystal orientation of the Si is <100>. If the cleaved pieces form triangles (cleave diagonally), then the crystal orientation of the Si is <111>.

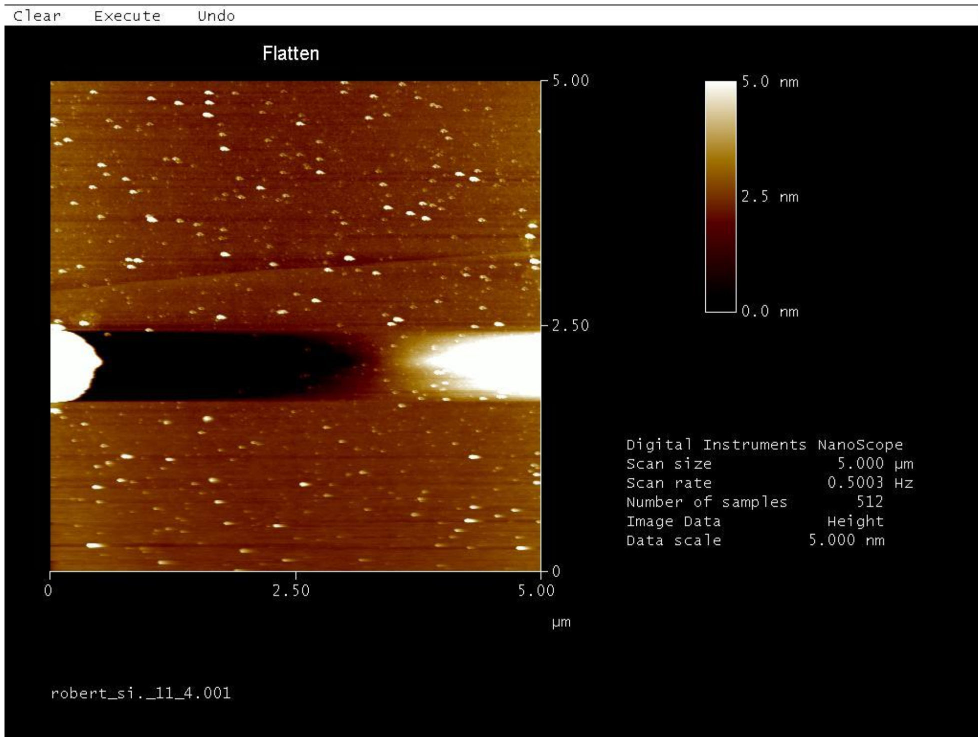
(5) Alternately, flat and secondary flat orientation may be compared to orientation conventions shown in the Semiconductor Technology Handbook.

IV - P-Type 4-inch Wafer Roughness Data

These are AFM images of P-type 4" prime wafers (below). These wafers are very smooth with the RMS roughness of around 2-4 angstroms. For each sample there are two 5 x 5 micron images, one entitled roughness analysis and the other entitled flatten.

The samples were cut from 4" p-type prime wafers, and diced by disco saw utilizing a 2-micron sacrificial photoresist layer. After the dicing, samples were washed in acetone, IPA and DI water, then atomic forced microscope (AFM) was used to measure the roughness.




Clear Execute Undo
Flatten
5.00
2.50
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0
2.50
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µm
5.0 nm
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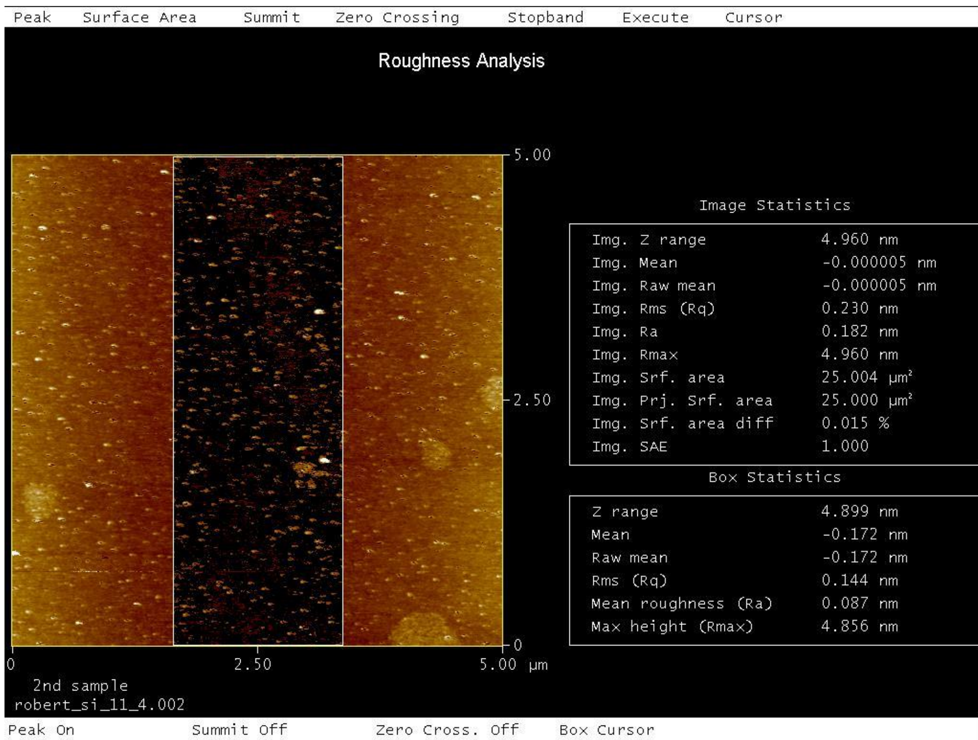
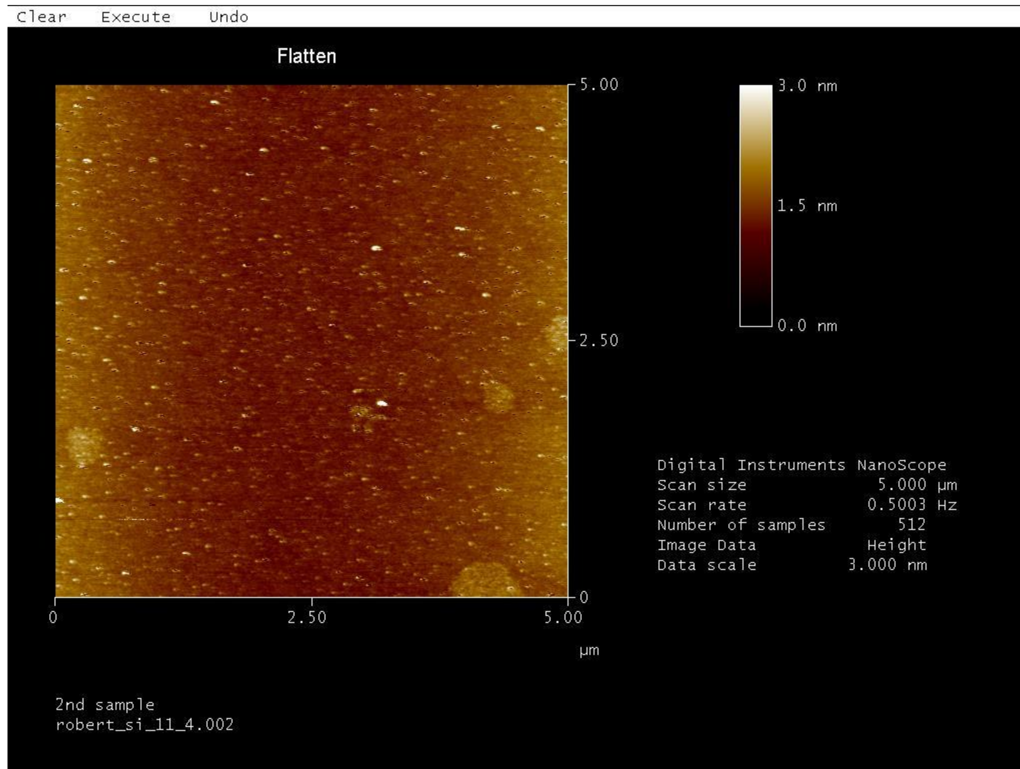
0.0 nm
Digital Instruments NanoScope
Scan size 5.000 µm
Scan rate 0.5003 Hz
Number of samples 512
Image Data Height
Data scale 5.000 nm
robert_si._11_4.001


Peak Surface Area Summit Zero Crossing Stopband Execute Cursor
Roughness Analysis
5.00
2.50
0
0
2.50
5.00 µm
Image Statistics
Img. Z range 4.960 nm
Img. Mean -0.000005 nm
Img. Raw mean -0.000005 nm
Img. Rms (Rq) 0.230 nm
Img. Ra 0.182 nm
Img. Rmax 4.960 nm
Img. Srf. area 25.004 µm²
Img. Prj. Srf. area 25.000 µm²
Img. Srf. area diff 0.015 %
Img. SAE 1.000
Box Statistics
Z range 4.899 nm
Mean -0.172 nm
Raw mean -0.172 nm
Rms (Rq) 0.144 nm
Mean roughness (Ra) 0.087 nm
Max height (Rmax) 4.856 nm
2nd sample
robert_si_11_4.002
Peak On Summit Off Zero Cross. Off Box Cursor



V – Trace Elements in 4”and 6” Prime and Test Wafers

WRS Materials, our supplier of 4” and 6” wafers provided an analysis of trace elements in their wafers.

Application Note:
Metals Testing

WRS Materials follows SEMI Spec guidelines in all three of our facilities for surface metals testing.

Below are the SEMI Spec requirements for surface metals according to SEMI M1 SPECIFICATIONS FOR POLISHED MONOCRYSTALLINE SILICON WAFERS.

SEMI Spec Requirements

Table 1: Suggested Polished Wafer Surface Metal Contamination Limits Appropriate to Circuits and Devices with a Minimum Linewidth in the Range of 0.8 – 1.2 µm

Elements	Contaminant Level
Sodium (Na), Aluminum (Al), Potassium (K), Chromium (Cr), Iron (Fe), Nickel (Ni), Copper (Cu)	Not greater than 1 x 10^{11} atoms/cm^2
Zinc (Zn)	Not greater than 1 x 10^{12} atoms/cm^2

Due to high measurement variability, data are recorded for process capability and not for individual shipment quality reports.

Technique & Methodology

WRS Materials tests these SEMI Spec guidelines by outsourcing wafers to ChemTrace, where the wafers undergo Vapor Phase Decomposition (VPD) inductively coupled plasma – mass spectrometry (ICP-MS).

Silicon wafers are placed in a pre-cleaned high purity chamber saturated with Hydrofluoric Acid (HF) vapor. The native or thermal oxide on the silicon wafer is dissolved in the presence of the HF vapor. Metal impurities incorporated into the oxide layer are released and dissolved in the acid during the scanning process.

A drop of an ultrapure acid etchant is added to the surface and the analysis area is scanned in a reproducible manner. The scanning solution is then collected for ICP-MS analysis.

Table 3: Typical Elements and Detection Limit for Surface Metals Analysis using VPD-ICPMS Method.

#	Element	Symbol	Method Detection Limit ($x10^{10}$ atoms/cm^2)	30 element analysis	13 element analysis
1.	Aluminum	(Al)	0.3	●	●
2.	Antimony	(Sb)	0.002	●	
3.	Arsenic	(As)	0.5	●	
4.	Barium	(Ba)	0.002	●	
5.	Beryllium	(Be)	0.2	●	
6.	Bismuth	(Bi)	0.001	●	
7.	Boron	(B)	5	●	
8.	Cadmium	(Cd)	0.003	●	
9.	Calcium	(Ca)	0.3	●	●
10.	Chromium	(Cr)	0.06	●	●
11.	Cobalt	(Co)	0.05	●	
12.	Copper	(Cu)	0.02	●	●
13.	Gallium	(Ga)	0.003	●	
14.	Germanium	(Ge)	0.01	●	
15.	Iron	(Fe)	0.1	●	●
16.	Lead	(Pb)	0.003	●	
17.	Lithium	(Li)	0.05	●	●
18.	Magnesium	(Mg)	0.1	●	●
19.	Manganese	(Mn)	0.03	●	
20.	Molybdenum	(Mo)	0.002	●	
21.	Nickel	(Ni)	0.05	●	●
22.	Potassium	(K)	0.2	●	●
23.	Sodium	(Na)	0.2	●	●
24.	Strontium	(Sr)	0.01	●	
25.	Tin	(Sn)	0.03	●	
26.	Titanium	(Ti)	0.05	●	●
27.	Tungsten	(W)	0.001	●	●
28.	Vanadium	(V)	0.01	●	
29.	Zinc	(Zn)	0.05	●	●
30.	Zirconium	(Zr)	0.01	●	

Capabilities

Currently the WRS San Jose, CA facility sends wafers out for trace metal analysis once a week and guarantee a metals spec of **<5E10 atoms/cm^2** for all metals listed in table 3.