Chapter 1.7

Material & Process Compatibility Policy

1.0 Title

Material & Process Compatibility Policy

2.0 Purpose

This document is designed to provide quick reference for material and compatibility policy in the NanoLab and will be visited by staff with updated information on a regular basis. This information complements the equipment manual chapter guidelines, should provide answer to some of the frequently asked questions about material and process compatibility in the NanoLab. The lab members are expected to contact staff for their "material and process compatibility" questions that may not be included in this chapter and/or covered by pertinent equipment chapters available at our website.

3.0 Scope

This chapter defines furnace pre-clean, rtp pre-clean, metal substrate/pyrex/borofloat glass restrictions in the NanoLab, as well as acceptable material in etchers and general use &VLSi sink definition table. This is a quick reference and by no means encompasses all the issues and concerns that may be raised about MOS, Non-MOS, as well as the General Sinks/PVD operation (582/582A) in the nanoLab. NanoLab users should adhere to specific guidelines spelled out in the operation manuals in addition to the information provided here to make their final decision on "what is allowed" and "what is not allowed" in certain area/s of the NanoLab/equipment. As always "ask when in doubt". Process engineering and/or operation manager should be consulted for any issues or concerns you may have in regards to "material and process compatibility". Furthermore, any new chemical or material introduced in the NanoLab must first be reviewed/approved by staff and the Material Data Sheet (MSDS) submitted to the front desk before taking it in the lab (soft copy of MSDS is preferred). A new MSDS form gets posted in one of the blue binders at the entrance of the NanoLab (gowning area). The MSDS forms are alphabetically arranged by their titles, provide an insight to what is considered new chemical or material in the NanoLab (not listed in these binders).

4.0 Applicable Documents

4.1 Chapter5 - Furnace and rtp chapters

4.2 Chapter7 - Etching system chapters

4.3 Chapter2 - Cleaning procedures and sink summary chapters

5.0 Definitions & Process Terminology

N/A

6.0 Safety

N/A

7.0 Statistical/Process Data

N/A

8.0 Available Process, Gases, Process Notes

Review specific equipment manual in addition to the policies outlined in Section 9.0.

9.0 Material and Process Policy (Cross-Contamination Prevention Measures)

9.1 VLSI Furnace, rtp and Sink Restrictions (Gold/highly diffusive materials restrictions)

No gold or highly diffusive materials are allowed in the VLSI area of the NanoLab, specifically in bay 386 where furnaces and rtp equipment are located, as well as majority of tools in the bay 384 (steppers, tracks), and some of the bay 584/586 equipment (Centura-Met, Centura MxP+, Lam etchers, and Centura-epi as it becomes available). Certain metals are allowed in specific furnaces, as described below. If you do not see your metal described there, discuss with staff before proceeding.

9.2 Basic Wafer Cleaning Policy (furnace pre-clean for silicon and 100% quartz (fused silica) wafers)

New wafers (out of vendor box) receive 1 piranha clean. Photoresist coated wafers need to have their PR stripped, then receive 2 piranha cleans (Non-MOS followed by MOS). Metal wafers (wafers with metal layer/s on them) should never be cleaned (dipped) in a piranha bath, as the sulfuric acid will attack the metal film and major contamination to the sink will occur.

- ► New 4" and 6" wafers must be cleaned in Msink6 piranha prior to loading into an MOS or Non-MOS furnace and rtp equipment in bay 386.
- ► Non-MOS processes will require additional piranha cleaning in Msink8.
- ► Resist coated 4" and 6" wafers with no metal layers on them, must be stripped with PRS3000 or O_2 plasma, and then cleaned in Msink8 piranha followed by Msink6 piranha clean, prior to loading into a MOS or Non-MOS furnace. This is true for both MOS and NON-MOS processes (2 Sink cleaning required).

9.3 Specialized Procedures for Furnace Processing of Metal-Coated Wafers

- ► Only specific metals are allowed in specific non-MOS furnaces.
- ► Do not attempt to clean any metal-coated wafers in any piranha bath.
- ► Metal wafers (wafers with metal layer/s) 4” & 6” wafers may be processed in specific non-MOS furnaces after being cleaned in the Msink1 metal clean bath followed by dump rinse (QDR) and SRD steps at Msink1 SRD station.
- ► Resist coated 4" & 6" metal wafers (wafers with metal layer/s) may be processed in specific non-MOS furnaces after resist stripping with PRS3000 and/or O_2 plasma, followed by cleaning in the Msink1 metal clean bath, then dump rinse (QDR) and SRD steps also done at Msink1 station.
- ► Non-MOS furnaces presently approved for processing of metal wafers (wafers with metal layer/s) are:
  - Tystar4 for annealing
  - Tystar12 for LTO
  - Tystar16 for amorphous or poly silicon deposition
  - Tystar17 for low stress nitride and HTO deposition
  - Tystar18 for sintering process
  - Tystar20 for poly-Ge/poly/SiGe film deposition.

9.4 Specialized Procedures for Furnace Processing of Non-quartz glass wafers

For information on different types of non-quartz glass wafers, see Process Module 31.Non-quartz glass wafers should Never be cleaned at Msink6.

- ► New 4" and 6" non quartz glass wafers must be cleaned in Msiink 8 piranha prior to loading into a Non-MOS furnace.

- ► Resist coated 4" and 6" non-quartz glass wafers, must be stripped with PRS3000 or O_2 plasma, and then cleaned in Msink8 piranha prior to loading into a Non-MOS furnace

9.5 Specialized Procedures for Rapid Thermal processing (rtp)

- ► Only specific metals are allowed in specific chambers in rtp1 (compound III-V with metal) and rtp3 (metals used for silicidation in the silicidation chamber that can be installed by request) and rtp4 (metals used for silicidation in the silicidation chamber, only).
- ► Do not attempt to clean any metal-coated wafers in any piranha bath.
- ► Metal wafers (wafers with metal layer/s) 4" & 6" wafers may be processed in rtp3 or rtp4 (silicidation chamber, only) after being cleaned in the Msink1 metal clean bath followed by dump rinse (QDR) and SRD steps at Msink1 SRD station.
- ► Resist coated 4" & 6" metal wafers (wafers with metal layer/s) may be processed in rtp3 or rtp4 (silicidation chamber, only), after resist stripping with PRS3000 and/or O_2 plasma, followed by cleaning in the Msink1 metal clean bath, then dump rinse (QDR) and SRD steps also done at Msink1 station.
- ► Process designation for rtp equipment detailed in chapter 5.30 and pertinent rtp chapters.
  - rtp1 - compound III-V semiconductor processing (activation/anneal and metal contact), as well as PZT processing in a separate chamber
  - rtp2 - activation/anneal of compound III-V semiconductor material (no metal allowed)
  - rtp3 - silicon based Non-MOS processes (silicidation chamber available upon request)
  - rtp4 - silicon based MOS activation/anneal & silicidation (separate chamber).
  - rtp8 - silicon based MOS gate oxide growth, silicon oxynitride and other electronic device related processes

9.6 Special Restriction on Etch Equipment

- ► No metal etching is allowed in Lam6 or Lam8. Use Lam7 (metal etcher) or Centura-MET for metal etch process.
- ► No glass (e.g.,Pyrex or borofloat) or quartz etching is allowed in Lam6, Lam7 and Lam8. Quartz as substrates can be used in lam6, Lam7 and Lam8 (100% SiO2 quartz). Non-quartz glass wafers may be etched in P-therm, Matrix-etch or STS-oxide at depth of few micron. See Chapter 1.3, Process Module 31 for more information.
- ► Do not grow C4F8 based polymers thicker than 1 micron in STS1 and STS2.
- ► No metal hard masks are allowed in the STS1, STS2 and STS –oxide, and Centura MXP machines. Use oxide/nitride and photoresist etch masks in STS1 and STS2 only.

9.7 Additional Information

Do not attempt etching Borofloat/Pyrex® wafers in **any** of the Lam etchers, Centura etchers, STS etchers and technics-c machine. **No etching of any type of glass wafers are allowed in these etchers in the NanoLab**, regardless of what film it is that you are trying to etch on your glass substrate.

Tystar 20 has specifically been developed to enable deposition of poly-Ge and poly-SiGe films on top of completed CMOS wafers. Therefore, expected metal contaminants in Tystar 20 may include, Al, Al2%Si, Ti, and W.

Furnace Pre-cleaning Requirement Table

Acceptable 4" and 6" and 8" substrates: Si, SOI, and quartz
(Non-quartz glass wafers (pyrex/borofloat) in Tystar4, Tystar16, Tystar12, and Tystar20, only)

		Pre-Cleaning Required for					
Equip.	**Description**	**New Si, SOI, Quartz Wafers**	**PR Coated Si, SOI, Quartz Wafers**	**New Non-Quartz Glass Wafers**	**PR Coated Non-Quartz Glass Wafers**	**Metal (blank film)**	**PR Coated Metal Wafers (See tube specific notes)**
Tystar1	**Atmos. Furnace (MOS)**	Msink6	**Restricted** See Tystar1 manual	NA	NA	NA	NA
Tystar2	**Atmos. Furnace (MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar3	**Atmos. Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar4	**Atmos. Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	Msink8	Wet Strip or Matrix + Msink8	Msink1 metal clean bath + Msink1 QDR/SRD *See Notes 1 and 2	Wet Strip or Matrix + Msink1 metal clean bath+ Msink1 QDR/SRD *See Notes 1 and 2
Tystar5	**Atmos. Furnace (MOS)**	Msink6	**Restricted** see Tystar1 manual	NA	NA	NA	NA
Tystar6	**Atmos. Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar7	**Atmos. Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar8	**Atmos. furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar9	**LPCVD Furnace (MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar10	**LPCVD Furnace (MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar11	**LPCVD Furnace (MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA

Tystar12	**LPCVD Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	Msink8	Wet Strip or Matrix + Msink8	Msink1 metal clean bath + Msink1 QDR/SRD *See Notes 1 and 2	Wet Strip or Matrix + Msink1 metal clean bath+ Msink1 QDR/SRD *See Notes 1 and 2
Tystar13	**Atmos. Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar14	**Atmos. Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar15	**LPCVD Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar16	**LPCVD Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	Msink8	Wet Strip or Matrix + Msink8	Sink1 metal clean bath + Sink1 QDR/SRD *See Notes 1	Wet Strip or Matrix + Msink1 metal clean bath+ Sink1 QDR/SRD *See Notes 1
Tystar17	**LPCVD Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	Msink1 metal clean bath + Msink1 QDR/SRD *See Notes 1	Wet Strip or Matrix + Msink1 metal clean bath+ Msink1 QDR/SRD *See Notes 1
Tystar18	**Atmos. Furnace (MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	Msink1 metal clean bath + Msink1 QDR/SRD +Msink8 SRD *See Notes 1 and2	Wet Strip or Matrix + Msink1 metal clean bath+ Msink1 QDR/SRD *See Notes 1 and 2
Tystar19	**LPCVD Furnace (MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	NA	NA	NA	NA
Tystar20	**LPCVD Furnace (Non-MOS)**	Msink6	Wet Strip or Matrix + Msink8 + Msink6	Msink8	Wet Strip or Matrix + Msink8	Msink1 metal clean bath + QDR+ SRD in Msink1 *See Notes 1 and 2	Wet Strip or Matrix + Msink1 metal clean bath+ Msink1 QDR/SRD *See Notes 1 and 2

Note 1: No metal wafers with melting points below 1500ºC are allowed in this furnace.

Note 2: Wafers with Al/2%Si allowed in this furnace.

Rapid Thermal Process(rtp) Pre-cleaning Requirement Table

Acceptable 4" and 6" and 8" substrates: Si, SOI, quartz
(Non-quartz glass wafers (pyrex/borofloat) in rtp1 only)

		Pre-Cleaning Required for					
Equip.	**Description**	**New Si, SOI, Quartz Wafers**	**PR Coated Si, SOI, Quartz Wafers**	**New Non-Quartz Glass Wafers**	**PR Coated Non-Quartz Glass Wafers**	**Metal (blank film)**	**PR Coated Metal Wafers**
rtp1	**Compound III-V and PZT**	**Recommended** Msink16 or Msink18 * See note1	**Restricted** ptherm resist ash or Msink2 wet strip + Msink16 or Msink18 * See note 1	**Recommended** Msink16 or Msink18 * See note 1	**Restricted** ptherm resist ash or Msink2 wet strip + Msink16 or Msink18 * See note 1	Msink16 or Msink18 * See note 1	**Restricted** ptherm resist ash or Msink2 wet strip + Msink16 or Msink18 * See note 1
rtp2	**Compound III-V no metals**	**Recommended** Msink16 or Msink18 * See note1	**Restricted** ptherm resist ash **+** Msink16 or Msink18 * See note1	**Recommended** Msink16 or Msink18 * See note 1	**Restricted** ptherm resist ash + Msink16 or Msink18 * see note1	N/A	N/A
rtp3	**Non-MOS silicon based processes**	Msink6	Matrix ash or Msink1 strip, + Msink8 and Msink6	Msink8	Matrix ash or Msink1 strip + Msink8	Msink1 metal clean * See Note2	Matrix ash + Msink1 metal clean
Rtp4	**MOS silicon based processes**	Msink6	Matrix ash or Msink1 strip, + Msink8 and Msink6	N/A	N/A	Msink1 metal clean * See Note2	Matrix ash + Msink1 metal clean
rtp8	**MOS silicon based gate oxidation, only**	Msink6	Matrix ash or Msink1 strip, + Msink8 and Msink6	NA	NA	NA	NA

Note1- Acetone or other clean steps such as; acetone, methanol and DI rinse can be applied to clean substrates at Msink16 & Msink18 - user discretion.
Note2 - Silicidation chamber and specific metals used for silicidation only.

Eth Equipment Table

Acceptable 4" and 6" substrates: Si, SOI, and quartz specific rules applied to glass and Quartz substrate etching

	Etcher Type	Pyrex® 7740 Etching	Pyrex® 7740 as substrate*	Quartz Etching	Quartz as substrate°
Lam6	Plasma	No	Yes[1]	No	Yes[1]
Lam7	RIE	No	Yes[1,2]	No	Yes[1,2]
Lam8	RIE	No	No	No	Yes[1,2]
STS1	DRIE	No	Yes[2]	No	Yes[2]
STS2	DRIE	No	Yes[2]	No	Yes[2]
STS-oxide	RIE	No	Yes[2]	Yes	Yes[2]
Technics-C	Plasma	No	No	No	Yes
Centura MxP+	RIE	No	No	Yes[1, 2]	Yes[1, 2]
Centura 3-5	RIE	No	Yes[1,2]	No	Yes[1, 2]
Centura MET	RIE	No	No	No	Yes[1, 2]
Centura Strip	Plasma	No	Yes[1]	No	Yes[1]
Semi	Plasma	No	No	No	Yes
Oxford	Plasma	No	No	No	Yes
Matrix	Plasma	No	Yes	No	Yes
Matrix_etch	Plasma	Yes	Yes	Yes	Yes
Ptherm	Plasma	Yes	Yes	Yes	Yes
AMST	RIE	No	Yes	No	Yes

IonMill	RIBE	Yes	Yes	Yes	Yes
Table continued,	**Etcher Type**	**Pyrex® 7740 Etching**	**Pyrex® 7740 as substrate***	**Quartz Etching**	**Quartz as substrate°**
primaxx	Non-plasma anhydrous HF VP	Yes[3]	Yes[3]	Yes	Yes
Xetch	Non-Plasma XeF_2 gas	No	Yes	No	Yes

[1] Lam6-8 and Centura machine use LED sensors at the indexer and edge detector units that cannot detect transparent substrates such as Pyrex® 7740 or Quartz. The sensors on Lam6-8 and Centura can usually handle transparent wafers with thin layer(s) of opaque films on them, i.e. amorphous polysilicon and/or metal layer.

[2] Equipment employs electrostatic chuck: additional conductive handle substrate necessary. A pure silicon handle wafer is required for this type of application.

[3] Material Controls: Mobile ion and diffusive noble metal containing substrates must use a proper carrier wafer. No germanium or PECVD Silicon Nitride is allowed in the chamber.

Note: Ptherm , Ionmill and Matrix-etch are the Nanolab tools in which members may attempt Pyrex® 7740 plasma etching.

- ► Pyrex® 7740 as substrate = there will be no exposed Pyrex® during plasma etch of some other material that has been deposited on a Pyrex® wafer.
- ► Quartz as substrate = there will be no exposed quartz during plasma etch of some other material that has been deposited on a quartz wafer.

VLSI and General Use Sink Definition Tables

Sink	Tank	Chemical Type Allowed	Wafers Processed			Spin Rinse Dryer	
			Pre-Clean Before		Wafers w/ PR	4"	6"
			MOS Furnace	Non-MOS Furnace			
Msink6 (MOS)	left heated tank	Piranha	yes	yes	no	SRD6 stack (Msink6)	SRD6 stack (Msink6)
	right heated tank	Piranha	yes	yes	no		
	left center-tank	25:1 HF	yes	yes	no		
	right center-tank	10:1 HF	yes	yes	no		
	left QDR	DI-water	yes	yes	no		
	right QDR	DI-water	yes	yes	no		
sink7 (General use)	left heated tank	Staff general use+ heated H2O2 for poly Ge etch	no	no	no	SRD8 stack (Msink8)	SRD8 stack (Msink8)
	right heated tank	phosphoric acid (Si3N4 etch only)	no	no	no		
	left center-tank	Silicon etch + general use, but no piranha/sulfuric (non-MOS)	no	no	yes		
	right center-tank	100:1 HF+ general use, but no piranha/sulfuric (MOS)	no	no	yes		
	left QDR	DI-water	no	no	yes		
	right QDR	DI-water	no	no	yes		
Msink8 (Non-MOS)	Left heated tank	Al etch	no	no	yes		
	center tank	5:1 BHF	no	no	yes		
	right heated tank	piranha (Non-MOS clean, also wafers post PR strip allowed)	no	no	no		
	left QDR	DI –water	no	no	yes		
	right QDR	DI- water	no	no	yes		

Note: No metals are allowed in Msink6, Msink7 and Msink8, except aluminum in aluminum etch bath at Msink8.

Sink	Tank	Chemical Type Allowed	Wafers Processed			Spin Rinse Dryer		
			Pre-Clean Before			4"	6"	8"
			MOS Clean Furnace	Non-MOS Clean Furnace	Wafers w/ PR			
Msink1 (General use)	Far left heated tank	Pre-Furnace clean (SVC-14)	no	no	no	SRDMsink1 stack (Msink1	SRDMsink1 stack (Msink1	SRDMsink1 stack (Msink1
	Center heated tank	PRS-3000	no	no	yes			
	Right heated tank	PRS-3000	no	no	yes			
	Front ambient bath	Developer solution	no	no	yes			
	Rear ambient bath	Developer solution	no	no	yes			
	Front rinse tank (QDR)	water	no	no	yes			
Msink3	Rinse tank and spin coater	water	no	no	yes	SRDMsink1	SRDMsink1	SRDMsink1
Msink2 (Note2)	Left rear heated tank	PRS-3000	no	no	yes	SRDMsink1 stack (Msink1	SRDMsink1 stack (Msink1	SRDMsink1 stack (Msink1
	Center rear heated tank	PRS-3000	no	no	yes			
	Right rear heated tank	Optional resist stripper	no	no	Yes			
	Left front rinse tank (QDR)	DI-water	no	no	Yes			
	General rinse	DI-water	no	no	Yes			
	Right glove wash	water	no	no	yes			
Msink4 (Non-MOS)	Left rear heated tank	KOH	no	no	no	SRDMsink1 stack (Msink1	SRDMsink1 stack (Msink1)	N/A
	Right rear heated tank	TMAH	no	no	no			
	Left front rinse tank (QDR)	DI-water	no	no	no			
	Right rinse tank	DI-water	no	no	no			
Msink5	HF release tank	HF	no	no	yes	N/A	N/A	N/A
	Cascade DI rinse	water	no	no	yes			
Msink16	Utility sink with gooseneck	water	no	no	yes	N/A	N/A	N/A
	Right glove wash	water	no	no	yes			
Masink18	Utility sink with gooseneck	water	no	no	yes	N/A	N/A	N/A

Note1 The Left tank in Msink1 is dedicated to Pre-furnace cleaning for metal wafers allowed in certain furnaces, as described in the above furnace table.

Note2 Msink2 is considered gold contaminated sink therefore wafers processed at this sink can not go into VLSI sinks and/or equipment

Note3 Masink16 and Msink18 are General Use Acid/Solvent sinks, therefore, do not have specific chemicals assigned to them